analog dialogue

A forum for the exchange of circuits and systems for test, measurement, and control

Volume 17, Number 1, 1983

ANALOG DEVICES

Editor's Notes

A & D—INSEPARABLE

You may ask: "Why is a journal with so much digital content still called "*Analog* Dialogue"?

The facile answer is that digital electronics is basically analog, since it deals in voltage and current; the *analog* values of signals establish their digital state. This argument gains some force when you consider that a digital signal—which arrives buried in noise—must first be recovered as an analog signal before the digital information in it (which may in turn represent the results of an analog measurement) can be interpreted.

You can also look at it historically. Ever since our op amps were first used to process analog signals for data acquisition, Analog Devices, Inc., has been involved in some aspect of the digital processing of analog signals. Our involvement increased as we successively (and successfully) engaged in the manufacture of a/d and d/a converters, data-acquisition systems, microcomputer I/O interface boards, computer-based measurement and control systems—and now, components and subsystems for DSP. The "analog" aspect of our mission continues to be the real-world origin of the signals being processed—and real-world signals are predominantly analog. *Conclusion*: When real-world signals must be processed, Analog and digital are inseparable.

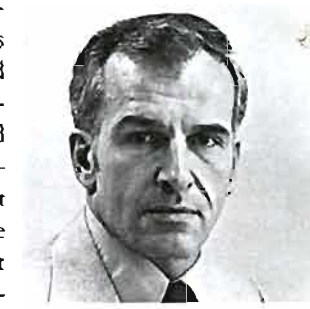
FATTENING UP THE DIALOGUE

If you're a typical reader, you've been reading *Analog Dialogue* for more than 2 years and are an E.E., working in measurement and control system design. When you read this magazine, you look first for applications articles but also have a strong interest in our new products. You don't think there's much room for improvement, but you do need more articles on signal conditioning, µP and µC interfacing, digital signal processing, op amps, and data-acquisition systems. The kinds of articles you need are mainly on practical matters (noise, grounding, etc.), but also include tutorials, applications ideas, applications by users (which you're always welcome to send to be considered), and cookbook examples. You're not much interested in technology or internal design of our products, unless it affects their application. You want *more*: more pages per issue, more issues per year, more material per article.

These are some of the things readers told us in a recent survey. We'd been eager to find out if our readers get what they want from *Analog Dialogue* and how we can do a better job. So we sent questionnaires with the last issue (16-3) to a random sampling of readers in the U.S. A sizeable proportion having been returned and analyzed, we've drawn this major conclusion: You have given us a mandate to increase the proportion of practical, tutorial, and idea-type articles. In order to do this without reducing the space devoted to technical information on new products (which you also want), we intend to gradually increase the total number of pages in each issue (which you also asked for). You asked for it? You've got it. ▶

Dan Sheingold

THE AUTHORS



A. Paul Brokaw (page 14) is a Division Fellow at Analog Devices Semiconductor. He has designed numerous successful ICs, including voltage references, ADCs, and amplifiers. His many activities include circuit design, new-product definition, contributions to the work of the Education-Support and Patent Committees, and mentoring. He has numerous patents and publications and is active in IEEE. He has a B.S. in Physics from Oklahoma State University.

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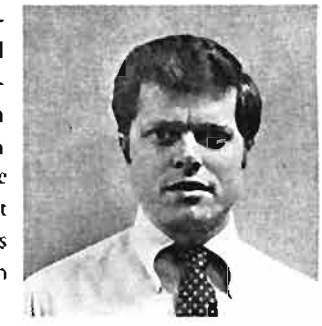

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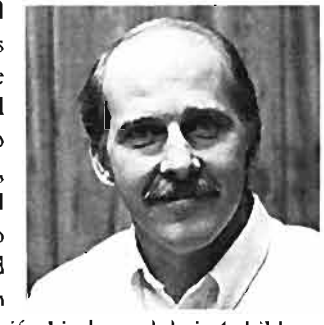

Jerry Neal (page 18) is a Regional Marketing Engineer at ADI's Computer Labs Division. A native of North Carolina, he attended N. C. State University. Prior to joining ADI, he invented, patented, and manufactured a soil moisture sensor; he has also worked for Hewlett Packard and Burroughs. He joined CLD in 1981, returning to N.C. with his wife, Linda, and their 4 children. They enjoy gardening and travel.

(Continued on page 26)

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LOW-POWER DIGITAL SIGNAL-PROCESSING ICs

Facilitate Filtering, FFT, Correlation, Averaging, and Much Else

8 X 8 and 16 X 16 Multipliers & Multiplier/Accumulators Dissipate <175 mW

by John Oxaal

The rapid growth of Digital Signal Processing (DSP) has led to a wealth of exciting new electronic end-products with a wide diversity of applications. The use of DSP has provided improved performance at lower cost in spectrum and analyzers, transmultiplexers, modems, medical imaging equipment, IC bonders, encryption devices, radars, and more. As the price of DSP circuits continues to fall—and especially in relation to what can be accomplished with them—and as engineers become more familiar with the techniques, we can look forward to a whole new generation of electronic equipment with significantly improved performance.

WHAT IS DSP?

Digital signal processing is not new. In its most general form, the term describes all of the operations that are done by and with digital logic circuitry and computers to condition or extract meaning from signals acquired in the real world. However, most computers process information sequentially, and they have difficulty performing timely and error-free number-crunching of large arrays of fast-changing data.

"DSP," in a more specialized meaning that has grown increasingly familiar—the sense in which we use it here—refers to techniques that enhance the computer's ability to process data rapidly and accurately, mainly by the introduction of hardware and firmware that provide the benefits of parallel processing. For some applications, a signal processor will be used in conjunction with a large mainframe to offload hairy computations and provide accelerated computing ability; at the other pole, the signal processor might constitute virtually the entire instrument, except for analog data-acquisition circuits, a certain amount of digital housekeeping furnished by a microprocessor, and—of course—user controls and display.

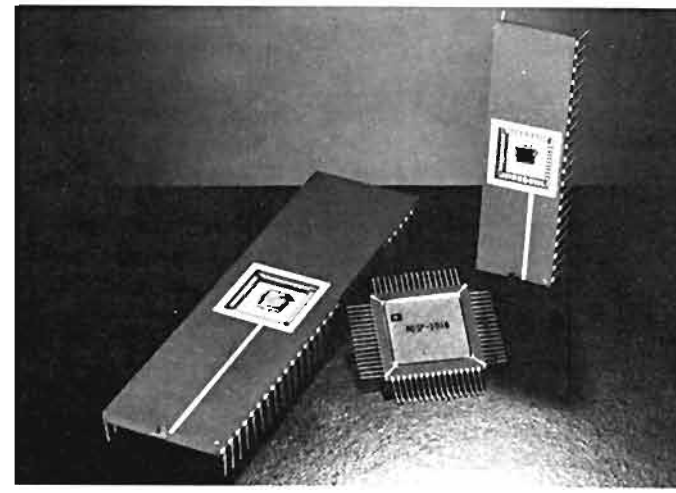
DSP, in an analogy to analog signal processing, consists of specialized techniques using high-performance circuits and programs that enable signals to be processed numerically at high speeds, often approaching real time, i.e., "analog speeds with digital accuracy."

Three of these techniques—filtering, correlation, and fast Fourier transformations (FFT)—comprise sixty or seventy percent of all current DSP practice. Another twenty percent involve matrix operations (multiplication or addition of two matrices) typically required for graphics and control. These techniques are briefly discussed in the following pages.

FILTERING, CORRELATION, AND FFT

Digital filters are used for exactly the same purposes as analog filters; to pass signals in certain frequency bands and to attenuate signals in other frequency bands. Modern digital filtering is carried out by performing the successive multiplications and additions required to perform convolution in the time domain—corresponding to multiplication in the frequency domain.

To understand how a digital filter works, remember that, in the



frequency domain, the spectrum of the input signal is multiplied by the frequency response function of the filter circuit to produce an output signal having a predetermined set of frequency components. You may recall that this multiplication in the frequency domain is equivalent to the convolution of two signals in the time domain, i.e., integration of the product of the folded input time function, $f(\tau-t)$, and an indicial response function, $g(t)$, with respect to time, to give a response which is a function of τ. An analog filter circuit automatically performs the convolution implied by its physical circuit architecture and coefficients to provide the (real) time-domain response, but manually computed response predictions are easier to perform in the frequency domain, using the classical continuous calculus.

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Digital signal processing, however, makes it possible to perform large numbers of accurate incremental calculations in a short time. In digital signal processing, difference calculus replaces differential calculus, and time-response of the filter can be calculated directly by convolution. The input signal is already available in the form of a sampled time function in suitable increments (for all values of τ), the indicial response function for each time increment can be computed initially and stored in memory, and integration is replaced by summation. With today's components, multiplication (16 bits × 16 bits) and addition can be performed rapidly (e.g., at 5-MHz rates), repeatedly, at low cost, and with low dissipation (less than 175 mW) and no drift.

A typical digital filtering process is illustrated by (1):

$$Y(n) = \sum_{m=0}^{n-1} H(m)\, X(n-m) \qquad (1)$$

Each output sample, Y(n), is obtained by multiplying m input samples, X(n − m), by m coefficients, H(m), and summing the results.

The filter coefficients, H(m), are weighted in the time domain so that, when transformed to the frequency domain, they describe the desired filter response. An ideal brick-wall low-pass filter, for example, is a square-wave in the frequency domain; thus the time-domain representation of its amplitude would be a (sin x)/x function of infinite duration. The H(m) would then be weighted according to a realizable approximation to that function. The convolving of the X(n-m) with the H(m) through equation 1 has the effect of multiplying the spectrum of the X(n-m) with that of the H(m). Since the frequency spectrum of the H(m) approximates the desired filter response, the Y(n) represent the correct values of time response appropriate to the filter characteristic and input waveshape.

Correlation is used to compare two signals, one of which is translated in time by a range of time delays. Auto-correlation compares a signal with delayed versions of the same signal; cross-correlation compares two different signals over a range of delay times. An algorithm for the digital implementation is

$$R(N) = \sum_{m=0}^{n-1} X(m)\, Y(m+N) \quad 0 < N \leq n-1 \qquad (2)$$

The degree to which X(m), the values of X at different times, m, are the same as the values of Y, Y(m + N), for a given delay time, N, determines the magnitude of R(N)—and thus the correlation between the two signals at time N − and provides a *correlation function* over all N, in the range 0 to n − 1.

As in the case of filtering, the algorithm employs a large number of successive multiplications and additions and is thus well suited for computation by DSP.

The *Discrete Fourier Transform*, very similar to the function performed by the more-efficient fast Fourier transform (FFT), is simply a sampled version of the Fourier transform where:

$$F(k) = \sum_{m=0}^{N-1} f(m)\, \epsilon^{-j2\pi mk/N} \qquad (3)$$

The transform variable, k, corresponds to frequency, m to time, and N is a normalizing factor. The Fourier components, F(k), of the Discrete Fourier Transform are equivalent to the H(w) of the continuous Fourier Transform shown below.

$$H(w) = \int_{-\infty}^{+\infty} h(t)\, \epsilon^{-jwt}\, dt \qquad (4)$$

The fast Fourier transform performs the same function as the discrete Fourier transform but is much more computationally efficient.

MATRICES

Modern graphics and control systems make extensive use of matrix multiplications. For example, to reduce the scale of an object on a graphics screen one must multiply the address of every point on the object by a number less than 1. To scale the point P(X,Y,Z)

$$P'(X,Y,Z) = P(X,Y,Z) \cdot S(S_x, S_y, S_z)$$

$$= [X,Y,Z,1] \cdot \begin{vmatrix} S_x & 0 & 0 & 0 \\ 0 & S_y & 0 & 0 \\ 0 & 0 & S_z & 0 \\ 0 & 0 & 0 & 1 \end{vmatrix}$$

$$P'(X,Y,Z) = [X \cdot S_x, Y \cdot S_y, Z \cdot S_z, 1] \qquad (5)$$

Similar operations abound in the control and graphics industries.

Note that each DSP technique requires multipliers, to multiply two variables, and/or multiplier-accumulators, to perform the multiplication and accumulate the sum of the products. Since the fastest microprocessors require about 5μs to perform a multiplication, their throughput rate—while performing the many repetitive operations called for by DSP—is quite slow. To enhance the speed of computation, dedicated peripheral devices operating at around 150ns per multiplication are required to obtain the throughput necessary for most of today's real-world signals. For this reason, multipliers are today the fundamental building block of DSP. Future unit device-functions for DSP will contain, in addition to multiplication, the on-chip memory, sequencing, and programming hooks necessary to perform the *complete* DSP algorithms shown above at considerably lower cost for comparable operations.

WHY USE DSP?

DSP is used to perform many of the same basic functions as analog signal processing. For example, analog filters and digital filters both pass signals in certain bands and attenuate signals outside that band. Digital signal processing, due to its higher cost, is used only when very high performance is required. For example, the 90th order FIR (finite impulse-response) filter transfer function shown in Figure 1 has a rolloff of 80dB/octave and can operate on 50kHz input signals. The phase response in the passband is linear.

The equivalent 13-pole analog filter would require at least seven op amps, many capacitors and resistors, and a long time to design. Moreover, the resulting filter would not be stable over time, temperature and power supply fluctuations; and to make it adjustable would be a near-impossible task.

Since the response of a digitally implemented filter is both stable and calculable—hence predictable—DSP is ideal for use in processors where stable implementation of very sharp rolloffs is required

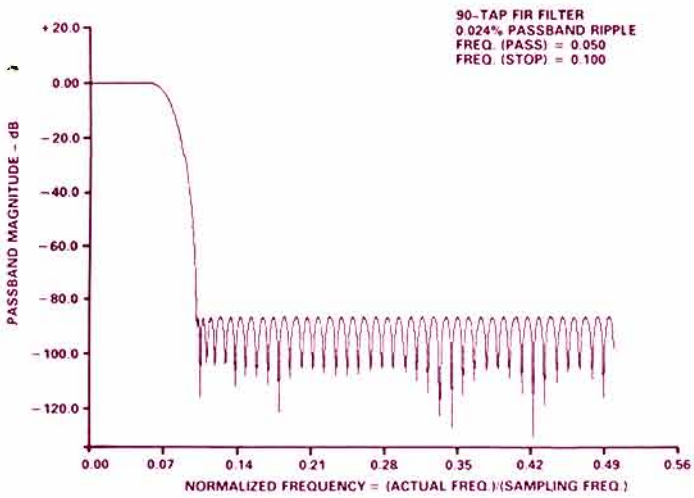


Figure 1. Normalized transfer function of 90-tap FIR filter having 0.024% passband ripple and 80dB/octave attenuation.

(e.g., spectrum analyzers and transmultiplexers) and/or where it is necessary to dynamically alter the transfer function of the system (e.g., adaptive filtering in the equalizer of a modem).

The advantages of digital signal processing in product development are substantial: prototype changes are commonly just software changes (high flexibility), and software simulation of the system will reflect the exact system performance. Simulation of analog systems cannot duplicate this precise correspondence. These advantages make DSP desirable in many applications where predictable performance is an inescapable requirement.

WHY IS ANALOG DEVICES BUILDING DSP CIRCUITS?

The declared business of Analog Devices is to develop components, subsystems, and systems for real-world signal processing, which includes measurement and control. The typical elements of a measurement-and-control loop, and the opportunities for digital signal processing, are shown in Figure 2. It is easy to see that DSP can offer powerful enhancements to this loop. For example, digital filtering could be used for noise reduction before the signal is processed, stored, or handled by the computer; and, for complex computations, an array processor could be used to provide accelerated computer performance.

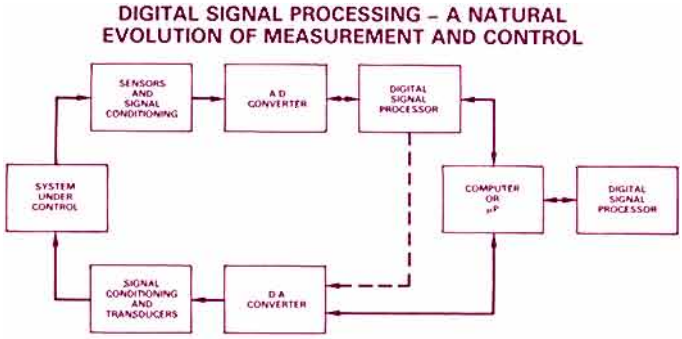


Figure 2. Signal processing in measurement and control.

In digital image-processing, the input to the DSP block would be video signals, and the output of the digital signal processor would drive a DAC that provides the intensity signal, as well as performing other functions, such as synchronization, etc. (We are already a major producer of video ADCs and DACs for those systems.)

Thus, DSP theory is a good fit to much of the signal handling in measurement and control, and video displays, which involve real-time signal processing. Also, our circuit-development and semiconductor-processing competences make it feasible to produce IC products to implement DSP theory at low cost and with low power consumption. Since DSP has such high potential applicability to our present measurement and control business, and DSP can now be economically implemented, and because our entry into the market as a competitor will clearly benefit all users of DSP—present and future—Analog Devices is making a strong commitment to the development, manufacture, and sale of products for DSP.

LOW POWER MULTIPLIERS AND MACS

As the first DSP fruits of our ten years of experience with CMOS, we have developed and manufactured the industry's first low-power CMOS multipliers and multiplier-accumulators. Four devices, pin-compatible second sources to industry-standard 8 × 8 and 16 × 16-bit multipliers and multiplier/accumulators, offer speed comparable to bipolar and NMOS devices but dissipate only ½0th as much power. Thus, as Figure 3 shows, we have minimized the designer's necessity for a speed/power tradeoff.

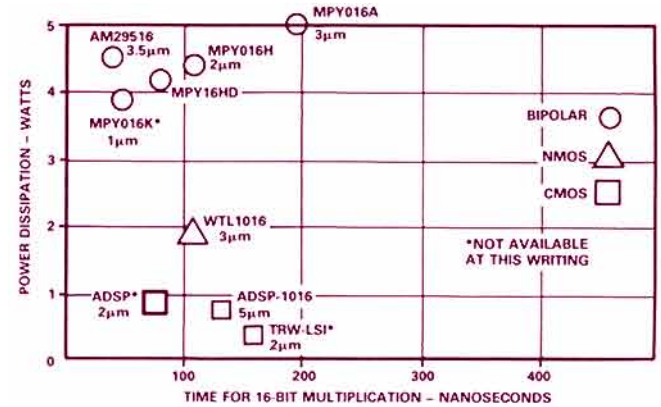


Figure 3. Dissipation vs. multiplying time for typical 16 × 16 multipliers.

The ADSP-1080* is an 8 × 8-bit multiplier with 100mW maximum power dissipation and 85-ns typical† multiplication time (compare: 1.65W and 65ns for the TDC-8HJ). The ADSP-1016* is a 16 × 16-bit multiplier with 150mW maximum power dissipation and 130-ns typical cycle time (cf. 4.5W and 100ns for the MPY-16J). Prices for commercial-grade ADSP's in ceramic DIPS are $45 (8 × 8) and $147 (16 × 16) in 100s.

A multiplier/accumulator that is pin-compatible with the TDC1008J, the 8 × 8-bit ADSP-1008* offers typical cycle time of 100 ns with 100-mW maximum power dissipation (vs. 70 ns and 2.15W). The ADSP-1010,* a 16 × 16 device that is pin-compatible with the TDC1010J multiplier/accumulator, specifies typical cycle time of 150 ns and maximum power dissipation of 175mW (vs. 120 ns and 5.5 W). Power dissipation specifications are guaranteed over the ADSPs' respective ambient temperature ranges. Prices for commercial grades in ceramic are $65 (8 × 8) and $198 (16 × 16) in 100s.

* For technical data use the reply card.
† 'Typical' means *maximum* multiplication time at 25°C.

Although slower at 25°C, the CMOS ADSPs' speed—temperature coefficient of 0.3% per °C (typical) results in speeds comparable to those of the older bipolar devices at +125°C. For example, at +125°C, 16 × 16 multiplication typically requires 175ns for the ADSP-1016, compared to 185ns for the MPY-16HJ. Furthermore, unlike devices with high dissipation, the cool-running CMOS ADSPs are specified at ambient still-air—rather than case—temperature. All models are available for both commercial and military temperature ranges, and the latter are available with processing to MIL-STD-883B; low power-dissipation also allows the devices to be offered in leaded chip carriers.

The ADSP devices are fabricated in a proprietary oxide-isolated bulk CMOS process employing an easily attained 5-μm feature size. High speed is achieved through such time-saving circuit techniques as: feedforward carry circuits, modified Booth algorithms and conditional-sum adders.

Figure 4 is a block diagram of the 8 × 8 ADSP-1080 CMOS multiplier. It consists of an asynchronous multiplier array, a pair of 8-bit input registers, a pair of 8-bit output registers, and control logic. The hard-wired multiplier array performs long multiplication, radix 2, much as you would do it with pencil and paper—but with additional tricks, mentioned above, to simplify and quicken the process. In order to avoid loss of accuracy in later computations due to roundoff error, all 16 output digits are preserved (multiplication can double the number of bits, for example, $(11 \times 11)_2 = 1001_2$).

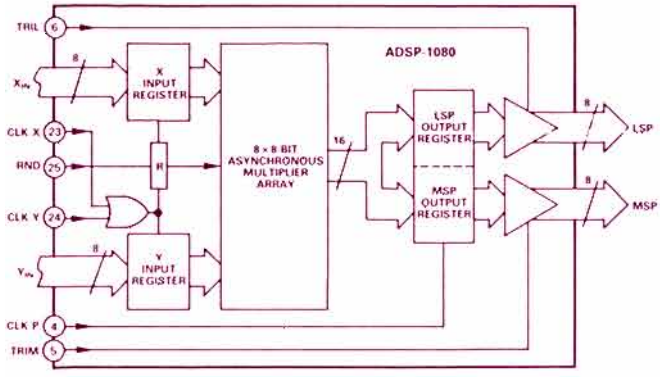


Figure 4. Block diagram of the 8×8 ADSP-1080 CMOS multiplier.

Figure 5 is a block diagram of the 16 × 16 ADSP-1010 multiplier-accumulator. Like a 16 × 16 ordinary multiplier, it has an asynchronous multiplier with a 32-bit output, two input registers, two product registers to accommodate the full product, and control logic. It also has an adder-subtractor to accumulate products and a 3-bit extended-product output register to avoid overflow when products are summed. Its least-significant-product output register shares a 16-bit bus with the Y-input register.

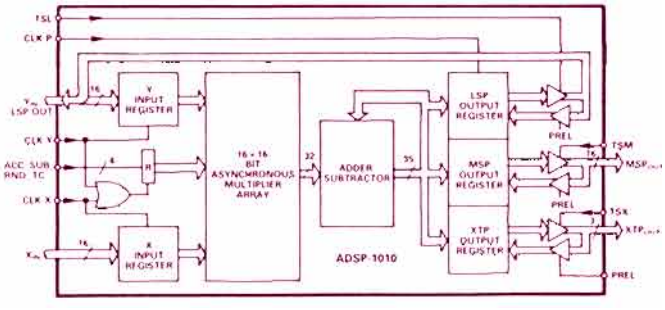


Figure 5. Block diagram of the 16 × 16 ADSP-1010 multiplier/accumulator.

APPLICATIONS

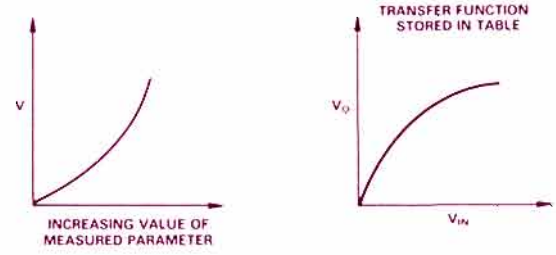
In digital filters, a succession of samples of the signal are multiplied by programmed constants and summed. If the samples include samples of the output, then the filter is *recursive*, and the output may continue to respond long after the input has reached equilibrium. This is an *infinite impulse response* filter. However, if the output depends only on the input samples, the output will always reach equilibrium at a finite time after the input has reached equilibrium; this is a finite-response (FIR) filter. Design techniques for the two types of filter differ, but as noted earlier, they involve multiplication and addition.

We've prepared a series of 5 articles comprising cookbook designs applying DSP to FIR (finite impulse-response) filtering, IIR (infinite impulse-response) filtering, digital heterodyning and decimation filtering, temporal averaging of images and waveforms, and implementation of modern control theory. These articles, all of them "meaty," were committed for publication in the trade press, started with EDN's March 3, 1983 issue. If you would like reprints of the articles (when available), use the reply card, specifying those topics of specific interest to you.

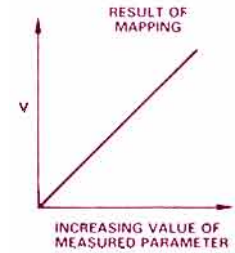
We have included here a relatively simple example in which digital signal processing is applied to a piecewise-linear-approximation interpolation method that substantially reduces the memory required to implement table lookups.

Piecewise-Linear Approximation

Often one has a need to perform a nonlinear transformation on a signal or data. For example, the calibration characteristics of a transducer can be nonlinear. The nonlinearity may be corrected for by adding a correction signal, multiplying by a correction factor, or mapping the inverse of the nonlinear function, as shown in Figure 6. To determine the inverse transformation over all input values, some form of storage of the function by analog or digital means is necessary.



(a) Nonlinear response. (b) Inverse function.



(c) Resulting overall linear function obtained by mapping (b) onto (a).

Figure 6. Nonlinearity correction by function fitting.

In analog circuitry, piecewise-linear function fitting is a time-honored approach to the generation of arbitrary nonlinear relationships between two variables,[1] since it was first used for simulation of nonlinearities in analog computing by G. A. Philbrick in the '40s. Although easy to implement for simple relationships and accuracies in the 0.2% to 5% range, it becomes unwieldy—if not impossible—when embodying relationships having many changes of slope and requiring precision to 0.01% or better.

In digital systems, where high speed of response is required, mapping the inverse function using a lookup table is an effective approach. However, large amounts of memory may be required if the highest resolutions and accuracies are to be obtained, especially if more than one function is involved. The most efficient approach in such circumstances may be to store a reasonable number of data points in memory for each function and perform fast interpolations with firmware.

Figure 7 shows a scheme employing piecewise-linear approximation. An input 16-bit word, X, is divided into two 8-bit bytes, X_i and ΔX, where i is any integer between 0 and 255, and ΔX lies between 0 and (1 - 255/256), in increments of $1/256$.

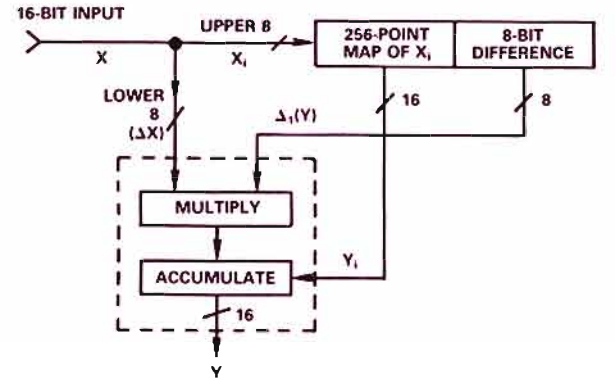


Figure 7. Configuration to obtain 16-bit function-fitting with 512 memory points, using piecewise-linear interpolation.

X_i, the number corresponding to the upper 8 bits of X, serves as an address to access two items of data stored in memory, Y_i, the value of Y corresponding to X_i, with 16-bit resolution, and the first difference, $\Delta_1(Y)$, the change in Y corresponding to a 1-bit increase in X_i. The relationships between these quantities are shown in Figure 8.

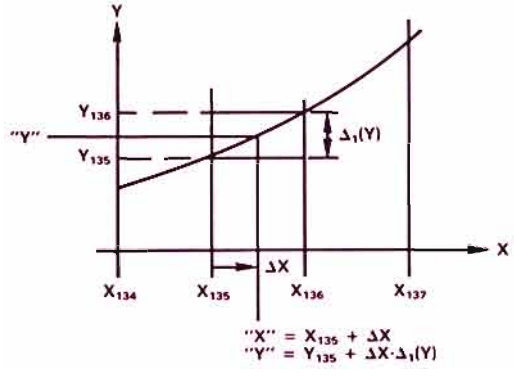


Figure 8. Graphical interpretation of interpolation.

The lookup table contains the value of the function at a given point and its first difference (Figure 9)

If you wish to interpolate linearly between the points, X_i, the new value of Y is given by

$$Y = Y_i + \Delta X \cdot \Delta_1(Y) \qquad (6)$$

As Figure 7 shows, ΔX, the lower 8 bits of X, and $\Delta_1(Y)$, from

X_i	Y_i	$\Delta_1(Y)$
X_0	Y_0	Y_1-Y_0
X_1	Y_1	Y_2-Y_1
⋮	⋮	⋮
X_{254}	Y_{254}	$Y_{255}-Y_{254}$
X_{255}	Y_{255}	—

Figure 9. Lookup table.

memory, are strobed into the lower 8 bits of X and Y, multiplied, and added to (or subtracted from) Y_i, which was preloaded from memory into the lowest 8 bits of the MSP register and the highest 8 bits of the LSP register, in an ADSP-1010 multiplier/accumulator, which, in effect, executes (6). An 8 × 8 multiplier, ADSP-1080, could be used, if sufficient time is available to use the microprocessor's accumulator to perform the addition.

Other means of interpolation are also available, to obtain a closer fit, or to perform the fit using a smaller number of memory points. For example, a quadratic approximation could be used, employing an additional multiplier or multiplier/accumulator, or—if time permits—a second multiplication with the same multiplier, using the system microprocessor for the housekeeping and addition. ◘

FOR FURTHER READING

In addition to the series of articles mentioned on page 6, available from ADI, the following publications may be helpful to the reader seeking more information about digital signal processing. *These publications are not available from Analog Devices.*

R. W. Hamming, *Digital Filters*, Second Edition (Englewood Cliffs, New Jersey: Prentice-Hall, 1983).

J. H. McClellan, T. W. Parks, and L. R. Rabiner, "A Computer Program for Designing Optimum FIR Linear-Phase Digital Filters," *IEEE Transactions on Audio and Electroacoustics*, Vol. AU-21, No. 8, December, 1973.

Alan V. Oppenheim and Ronald W. Schafer, *Digital Signal Processing* (Englewood Cliffs, New Jersey: Prentice-Hall, 1975).

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SHIELDING AND GUARDING

How to Exclude Interference-Type Noise
What to Do and Why to Do It—A Rational Approach

by Alan Rich

This is the second of two articles dealing with interference noise. In the last issue of *Analog Dialogue* (Vol. 16, No. 3, pp. 16-19), we discussed the nature of interference, described the relationship between sources, coupling channels, and receivers, and considered means of combatting interference in systems by reducing or eliminating one of those three elements.

One of the means of reducing noise coupling is *shielding*. Our purpose in this article is to describe the correct uses of shielding to reduce noise. The major topics we will discuss include noise due to capacitive coupling, noise due to magnetic coupling, and driven shields and guards. A set of guidelines will be included, with do's and don'ts.

From the outset, it should be noted that shielding problems are always rational and do not involve the occult; but they are not always straightforward. Each problem must be analyzed carefully. It is important first to identify the noise source, the receiver, and the coupling medium. Improper shielding and grounding, based on faulty identification of any of these elements, may only make matters worse or create a new problem.

You can think of shielding as serving two purposes. First, shielding can be used to confine noise to a small region; this will prevent noise from extending its reach and getting into a nearby critical circuit. However, the problem with such shields is that noise captured by the shield can still cause problems if the return path the noise takes is not carefully planned and implemented by understanding of the ground system and making the connections correctly.

Second, if noise is present in a system, shields can be placed around critical circuits to prevent the noise from getting into sensitive portions of the circuits. These shields can consist of metal boxes around circuit regions or cables with shields around the center conductors. Again, where and how the shields are connected is important.

CAPACITIVELY COUPLED NOISE

If the noise results from an electric field, a shield works because a charge, Q_2, resulting from an external potential, V_1, cannot exist on the interior of a closed conducting surface (Figure 1).

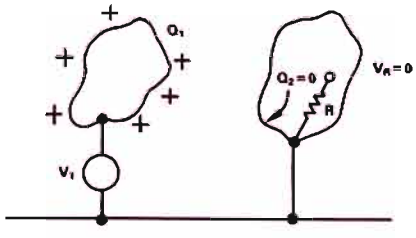


Figure 1. Charge Q_1 cannot create charge inside a closed metal shell.

Coupling by mutual, or stray, capacitance can be modeled by the circuit of Figure 2. Here, V_n is a noise source (switching transistor, TTL gate, etc.), C_s is the stray capacitance, Z is the impedance of a receiver (for example, a bypass resistor connected between the input of a high-gain amplifier and ground), and V_{no} is the output noise developed across Z.

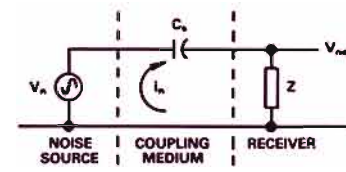


Figure 2. Equivalent circuit of capacitive coupling between a source and a nearby impedance.

A noise current, $i_n = V_n/(Z + Z_{Cs})$, will result, producing a noise voltage, $V_{no} = V_n/(1 + Z_{Cs}/Z)$. For example, if C_s = 2.5 pF, Z = 10kΩ (resistive), and V_n = 100mV at 1.3 MHz, the output noise will be 20 mV (0.2% of 10V, i.e., 8 LSBs of 12 bits).

It is important to recognize the effect that very small amounts of stray capacitance will have on sensitive circuits. This becomes increasingly critical as systems are being designed to combine circuits operating at lower power (implying higher impedance levels), higher speed (implying lower nodal stray capacitance, faster edges, and higher frequencies), and higher resolution (much less output noise permitted).

When a shield is added, the change to the situation of Figure 2 is exemplified by the circuit model of Figure 3. With the assumption that the shield has zero impedance, the noise current in loop A-B-D-A will be V_n/Z_{Cs1}, but the noise current in loop D-B-C-D will be zero, since there is no driving source in that loop. And, since no current flows, there will be no voltage developed across Z. The sensitive circuit has thus been shielded from the noise source, V_n.

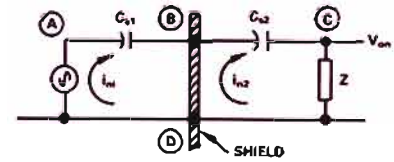


Figure 3. Equivalent circuit of the situation of Figure 2, with a shield interposed between the source and the impedance.

Guidelines for Applying Electrostatic Shields

- An electrostatic shield, to be effective, should be connected to the reference potential of any circuitry contained within the shield. If the signal is earthed or grounded (i.e., connected to a metal chassis or frame, and/or to earth), the shield must be earthed or grounded. But grounding the shield is useless if the signal is not grounded.
- The shield conductor of a shielded cable should be connected to the reference potential at the signal-reference node (Figure 4).
- If the shield is split into sections, as might occur if connectors are used, the shield for each segment must be tied to those for the

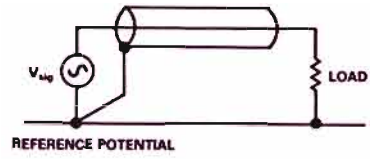


Figure 4. Grounding a cable shield.

adjoining segments, and ultimately connected (only) to the signal-reference node (Figure 5).

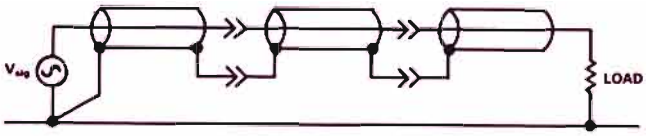


Figure 5. Shields must be interconnected if interrupted.

•The number of separate shields required in a system is equal to the number of independent signals that are being measured. Each signal should have its own shield, with no connections to other shields in the system, unless they share a common reference potential (signal "ground"). If there is more than one signal ground (Figure 6), each shield should be connected to its own reference potential.

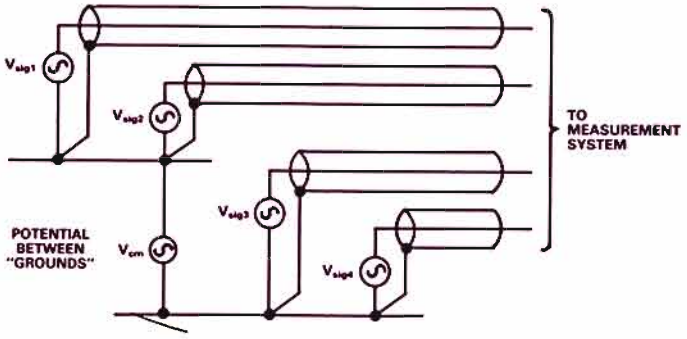


Figure 6. Each signal should have its own shield connected to its own reference potential.

•*Don't connect both ends of the shield to "ground"*. The potential difference between the two "grounds" will cause a shield current to flow (Figure 7). The shield current will induce a noise voltage into the center conductor via magnetic coupling. An example of this can be found in Part 1 of this series, *Analog Dialogue* 16-3, page 18, Figure 10.

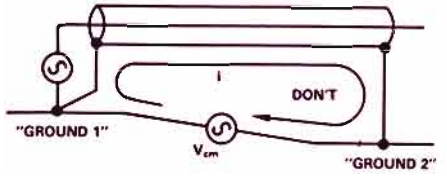
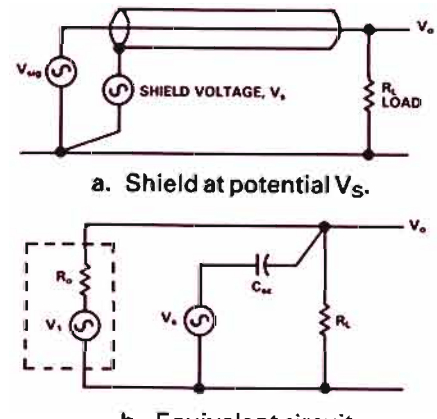


Figure 7. Don't connect the shield to ground at more than one point.

•*Don't allow shield current to exist* (except as noted later in this article). The shield current will induce a voltage in the center conductor.

•*Don't allow the shield to be at a voltage with respect to the reference potential* (except in the case of a guard shield, to be described). The shield voltage will couple capacitively to the center conductor (or conductors in a multiple-conductor shield). With a noise voltage, V_s, on the shield, the situation is as shown in Figure 8.



a. Shield at potential V_S.

b. Equivalent circuit.

Figure 8. Don't permit the shield to be at a potential with respect to the signal.

The fraction of V_s appearing at the output will be

$$V_o = \frac{V_s}{\sqrt{1 + \frac{1}{(2\pi f R_{eq} C_{sc})^2}}} \qquad (1)$$

where V_1 is the open-circuit signal voltage, R_o is the signal's source impedance, C_{sc} is the cable's shield-to-conductor capacitance, and R_{eq} is the equivalent parallel resistance of R_o and R_L. For example, if V_s = 1V at 1.5MHz, C_{sc} = 200pF (10 feet of cable), R_o = 1000 ohms, and R_L = 10kΩ, the output noise voltage will be 0.86 volts.

This is an often-ignored guideline; serious noise problems can be *created* by inadvertently applying undesired potentials to the shield.

•*Know by careful study how the noise current that has been captured by the shield returns to "ground."* An improperly returned shield can cause shield voltages, can couple into other circuits, or couple into other shields. The shield return should be as short as possible to minimize inductance.

Here is an example that illustrates the problems that can arise in relation to these last two guidelines: Consider the improperly configured shield system shown in Figure 9, in which a precision voltage source, V1, and a digital logic gate share a common shield connection. This situation can occur in a large system where analog and digital signals are cabled together.

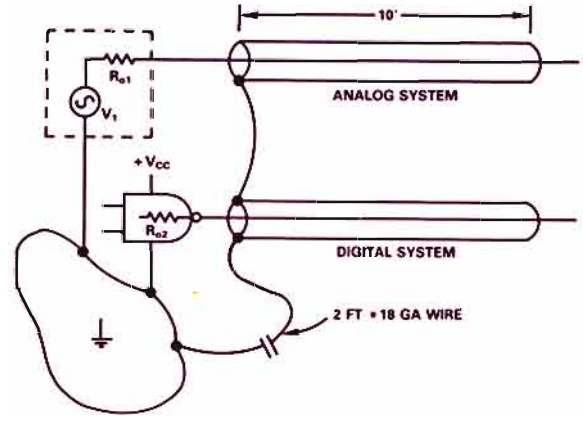


Figure 9. A situation that generates transient shield voltages.

A step voltage change in the output of the logic circuit couples capacitively to its shield, creating a current in the common 2-foot

shield return. This, in turn, develops a shield voltage common to both the analog and digital shields. An equivalent circuit is shown in Figure 10, in which V(t) is a 5-volt step from a TTL logic gate, R_{o2} is the 13-ohm output impedance of the logic gate, C_{ws} is the 470-pF capacitance from the shield to the center conductor of the shielded cable, and R_s and L_s are the 0.1-ohm resistance and 1-microhenry inductance of the 2-foot wire connecting the shield to the system ground.

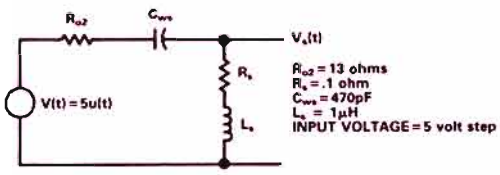


Figure 10. Equivalent circuit for generating shield voltage.

The shield voltage, $V_s(t)$, can be solved for by conventional circuit-analysis techniques, or simulated by actually building and carefully making measurements on a circuit with the given parameters. For the purpose of demonstration, the calculated response waveform, illustrated in Figure 11, with a 5-volt initial spike, resonant frequency of 7.3 MHz, and damping time constant of 0.15μs, is sufficient to illustrate the nature of the voltage that appears on the shield and is capacitively coupled to the analog input. If the voltage is looked at with a wideband oscilloscope, it will look like a noise "spike." We can see that this transient will couple a fast damped waveform of significant peak amplitude to the analog system input.

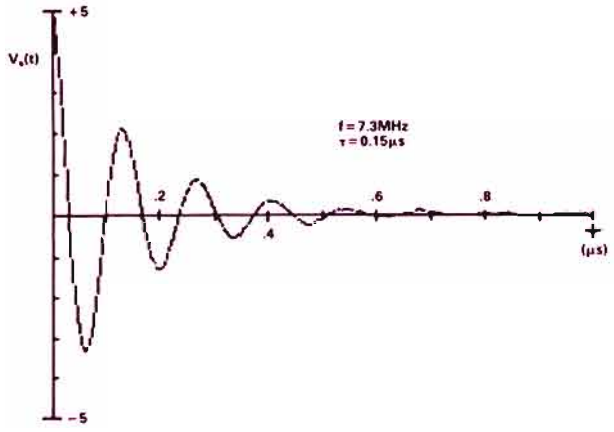


Figure 11. Computed response of circuit of Figure 10.

Even in a purely digital system, noise glitches can be caused to appear in apparently remote portions of a system having the kind of situation shown. This can often explain some otherwise inexplicable system bugs.

In quite a few cases, the proper choice of shield connection among the many possibilities may not be immediately obvious, and the guidelines may not provide us with a clear choice. There is no alternative but to analyze the various possibilities and choose the approach for which the lowest noise may be calculated.

For example, consider the case illustrated in Figure 12, in which the measurement system and the source have differing ground potentials. Should we connect the shield to A: the low side at the measurement-system input, B: ground at the system input, C: ground at the signal source, or D: the low side at the source?

A is a poor choice, since noise current is allowed to flow in a signal

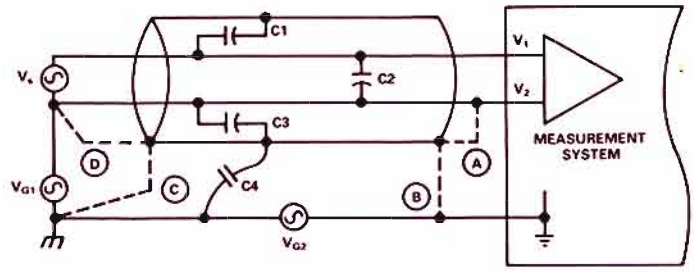


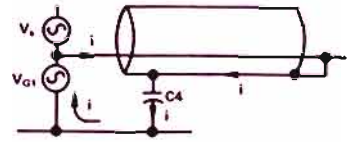
Figure 12. Possible grounds where system and source have differing ground potentials.

conductor. The path of the noise current due to V_{G1}, as it returns through C4, is shown in Figure 13a.

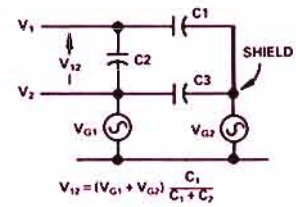
B is also a poor choice, since the two noise sources in series, V_{G1} and V_{G2}, produce a component across the two signal wires, developed by the source impedance in parallel with C_2, in series with C_1, as shown in Figure 13b.

C is poor, too, since V_{G1} produces a voltage across the two signal wires, by the same mechanism as (B), as Figure 13c shows.

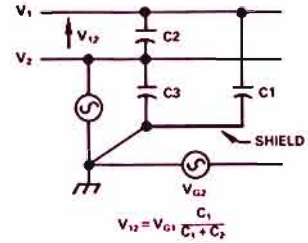
D is the best choice, under the given assumptions, as can be seen in Figure 13d. It also tends to confirm the grounding guideline to connect the shield at the signal's reference potential.



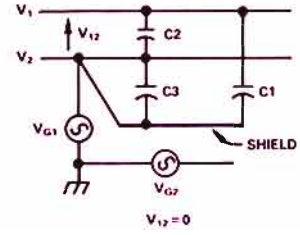
a. Return path A.



b. Return path B.



c. Return path C.



d. Return path D.

Figure 13. Equivalent circuits.

NOISE RESULTING FROM A MAGNETIC FIELD

Noise in the form of a magnetic field induces voltage in a conductor or circuit; it is much more difficult to shield against than elec-

tric fields because it can penetrate conducting materials. A typical shield placed around a conductor and grounded at one end has little if any effect on the magnetically induced voltage in that conductor.

As a magnetic field, B, penetrates a shield, its amplitude decreases exponentially (Figure 14). The skin depth, δ, of the shield material, is defined as the depth of penetration required for the field to be attenuated to 37% (exp (-1)) of its value in free air. Table 1[1] lists typical values of δ for several materials at various frequencies. You can see that any of the materials will be more effective as a shield at high frequency, because δ decreases with frequency, and that steel provides at least an order of magnitude more effective shielding at any frequency than copper or aluminum.

Figure 14. Magnetic field in a shield as a function of penetration depth.

Figure 15 compares absorption loss as a function of frequency for two thicknesses of copper and steel. ⅛-inch steel becomes quite effective for frequencies above 200 Hz, and even a 20-mil (0.5 mm) thickness of copper is effective at frequencies above 1 MHz. However, all show a glaring weakness at lower frequencies, including 50-60-Hz line frequencies—the principal source of magnetically coupled noise at low frequency.

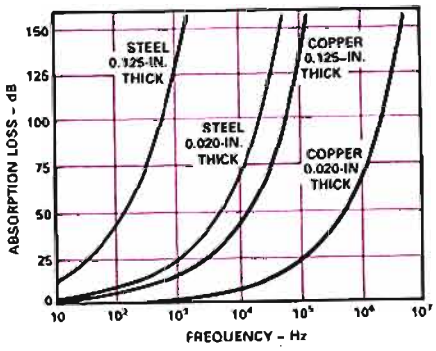


Figure 15. Absorption loss vs. frequency for two thicknesses of copper and steel.

For improved low-frequency magnetic shielding, a shield consisting of a high-permeability magnetic material (e.g., Mumetal) should be considered. Figure 16 compares a 30-mil thickness of Mumetal with various materials at several frequencies. It shows that, below 1 kHz, Mumetal is more effective than any of the other materials, while at 100kHz it is the least effective. However, Mumetal is not especially easy to apply, and if it is saturated by an excessively strong field, it will no longer provide an advantage.

Table 1. Skin depth, δ, vs. frequency

Frequency	δ for Copper (in.)	δ for Copper (mm)	δ for Aluminum (in.)	δ for Aluminum (mm)	δ for Steel (in.)	δ for Steel (mm)
60Hz	0.335	8.5	0.429	10.9	0.034	0.86
100Hz	0.260	6.6	0.333	8.5	0.026	0.66
1kHz	0.082	2.1	0.105	2.7	0.008	0.2
10kHz	0.026	0.66	0.033	0.84	0.003	0.08
100kHz	0.008	0.2	0.011	0.3	0.0008	0.02
1MHz	0.003	0.08	0.003	0.08	0.0003	0.008

[1]Table 1 and Figures 15 and 16 are from Ott, H.W., *Noise Reduction Techniques in Electronic Systems* (New York: John Wiley & Sons, © 1976).

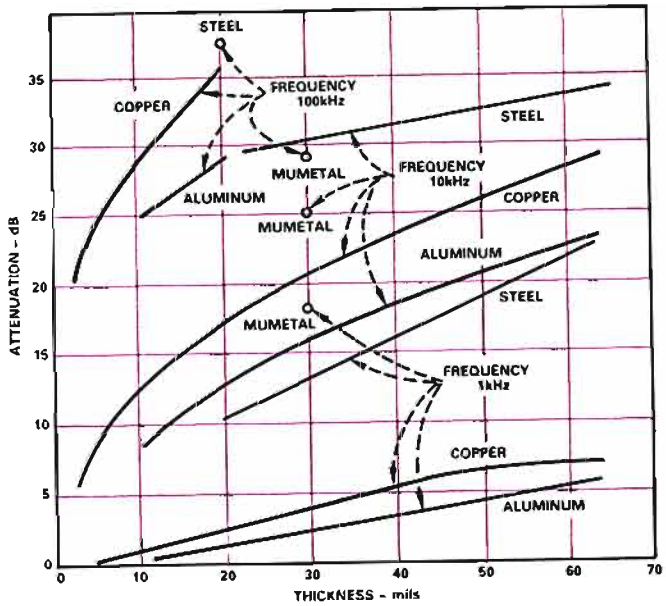
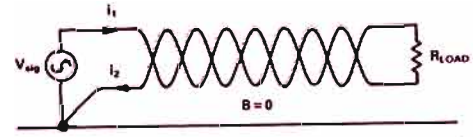


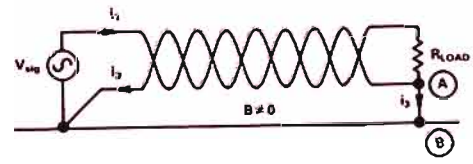
Figure 16. Shielding attenuation of Mumetal and other materials at several frequencies.

As you can see, it is very difficult to shield against magnetic fields, i.e., to modify the coupling medium by shielding. Therefore, the most effective approaches at low frequency are to minimize the strength of the interfering magnetic field, minimize the receiver loop area, and minimize coupling by optimizing wiring geometries. Here are some guidelines:

- Locate the receiving circuits as far as possible from the source of the magnetic field.
- Avoid running wires parallel to the magnetic field; instead, cross the magnetic field at right angles.
- Shield the magnetic field with an appropriate material for the frequency and field strength.
- Use a twisted pair of wires for conductors carrying the high-level current that is the source of the magnetic field. If the currents in the two wires are equal and opposite, the net field in any direction



a. Correct connection with balanced currents.



b. Incorrect connection forming ground loop.

Figure 17. Connections to a twisted pair.

over each cycle of twist will be zero (Figure 17a). For this arrangement to work, none of the current can be shared with another conductor, for example, a ground plane. Figure 17b shows what can happen if a ground loop is formed; if part of the current flows through the ground plane (depending on the ratio of conductor resistance to ground resistance), it will form a loop with the twisted pair, generating a field determined by $i_3 (= i_1 - i_2)$.

The ground connection between A and B need not be as simple as a short circuit to cause trouble. Any stray unbalanced capacitance or resistance from R_{load} circuits to the ground plane will also unbalance the currents and produce a net current through the wires and the ground plane, producing a ground loop and a related magnetic field. For this reason, it is also good practice to run the twisted pair close to the ground plane to tend to balance the capacitances from each side to ground, as well as to minimize loop area.

•Use a shielded cable with the high-level source circuit's return current carried in the shield (Figure 18). If the shield current, I_2 is equal and opposite to that in the center conductor, the center-conductor field and the shield field will cancel, producing a zero net field. In this case, which seems to violate the "no shield current" rule for receiver circuits, the concentric cable is not used to shield the center lead; instead, the geometry produces cancellation.

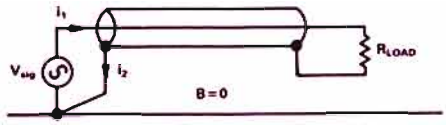


Figure 18. Use of shield for return current to noisy source.

This scheme can be usefully employed in an ATE system where accurate measurements must be performed on devices with high power-supply currents that may be noisy. For example, Figure 19 shows the application of this technique to the connections for the high-current logic supply for an a/d converter under test—at the end of a test cable.

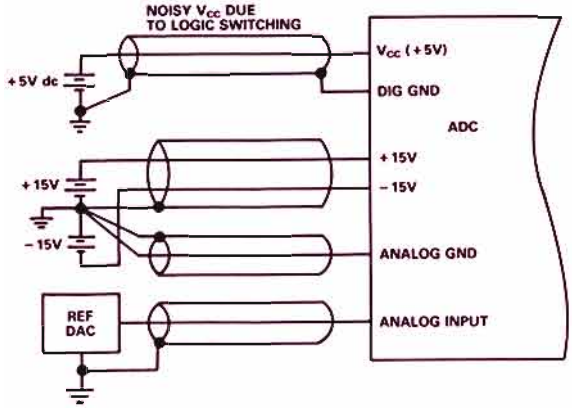


Figure 19. Application of circuit of Figure 18 in a test system.

•Since magnetically induced noise depends on the area of the receiver loop, the induced voltage due to magnetic coupling can be reduced by reducing the loop's area. What is the receiver loop? In the example shown in Figure 20, the signal source and its load are connected by a pair of conductors of length L and separation D. The circuit (assuming it has a rectangular configuration) forms a loop with area D · L.

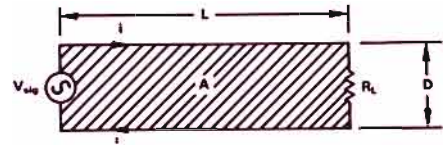


Figure 20. Area of a loop that receives magnetically coupled noise.

The voltage induced in series with the loop is proportional to the area and the cosine of its angle to the field. Thus, to minimize noise, the loop should be oriented at right angles to the field, and its area should be minimized.

The area can be reduced by decreasing the length of and/or decreasing the distance between the conductors. This is easily accomplished with a twisted pair, or at least a tightly cabled pair, of conductors. It is good practice to pair conductors so that the circuit wire and its return path will always be together. To do this, the designer must be certain of the actual path that the return current takes in getting back to the signal source. Quite often, the current returns by a path not intended in the original design layout.

If wires are moved (for example, by a technician troubleshooting some other problem), the loop area and orientation to the field may change, so that yesterday's acceptable noise level may be transformed to tomorrow's disastrous noise level. Which may lead to a service call . . . and another repetition of the cycle. The bottom line: Know the loop area and orientation, do what must be done to minimize noise—*and permanently secure the wiring*!

DRIVEN SHIELDS AND GUARDING

We have discussed the role of a current-driven shield carrying an equal and opposite current to reduce generated noise by reducing the magnetic field around a conductor.

Guarding is similar, in that it involves driving a shield, at low impedance, with a potential essentially equal to the common-mode voltage on the signal wire contained within the shield. Guarding has many useful purposes: It reduces common-mode capacitance, improves common-mode rejection, and eliminates leakage currents in high-impedance measurement circuits.

Figure 21 shows an example of an op amp with negligible bias current connected as a high-impedance non-inverting amplifier with gain. The purpose of the cable is to shield the high input-impedance signal conductor from capacitively coupled noise and to minimize leakage currents. The signal comes from a 10-megohm source, and the cable is assumed to have 1000 megohms of leakage resistance (which may change as a function of temperature, humidity, etc.) from conductor to shield. If connected as shown, the equivalent input circuit is an attenuator which loses 1% of the

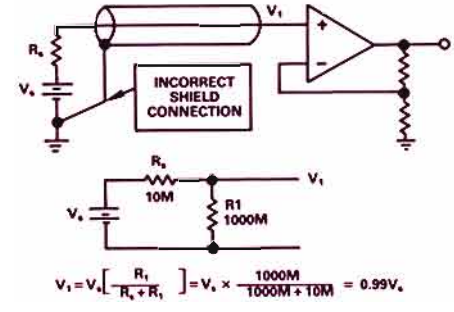


Figure 21. Op amp connected as high-impedance noninverting amplifier with gain, with shielded input lead.

signal at the time it is measured, and an unknown fraction at other times. Also, the cable capacitance produces a substantial lag time constant, R_sC_c.

Figure 22 has the same players, but the shield is connected to the tap of the gain divider (usually at low impedance). Being connected to the inverting input of the op amp, it should be at the same potential as the amplifier's non-inverting input. Since there is no voltage across the cable's leakage resistance, there is no current through it and its resistance value doesn't matter; V_1 must therefore be equal to V_s, since bias current was assumed negligible.

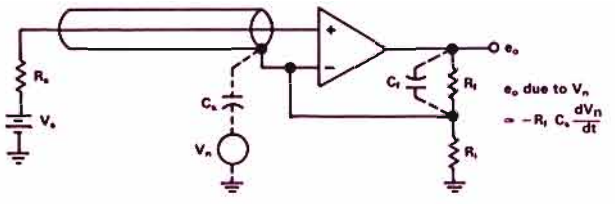
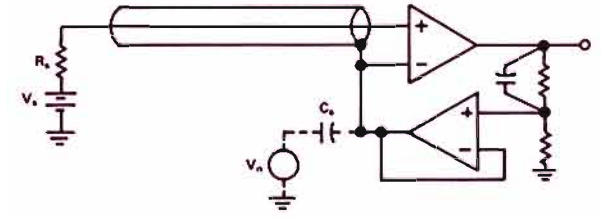


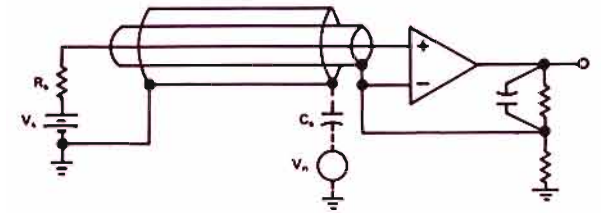
Figure 22. Same as Figure 21, but cable shield connected as a guard.

Also, there is no voltage across the cable capacitance, hence no charging or discharging of the cable; thus the lag time constant depends mainly on circuit strays and the amplifier's input capacitance. For stability, capacitance should be connected between the output and the negative input, such that $C_fR_F = C_sR_i$, where C_s is sum of the stray capacitance between shield and ground and the input capacitance.

There must be no noise voltage applied to the guard. In noisy systems, as Figure 22 shows, capacitively coupled noise will be differentiated, emphasizing the higher-frequency components. This can be avoided (Figure 23) by either using a buffer follower with fast response and low output impedance to drive the guard (a) or a second shield, around the guard, grounded to the signal common (b).



(a) Driven guard.



(b) Shielded guard.

Figure 23. Avoiding noise pickup on the guard.

In high-impedance current-input inverting configurations, where a length of shielded wire is used to guard the lead from the current source to the amplifier's inverting input, the guard should either be driven by a buffer at the same potential as the non-inverting input (and connected nowhere else), or be tied directly to the non-inverting input, with a second outer shield connected to the signal's reference point.

SUMMARY

Table 2 summarizes the important points made in this article. All are important to maintaining a high-integrity shield system. However, we cannot emphasize too strongly the two subjects that are most-often ignored: appearance of noise voltage on signal shields and proper disposition of shield noise currents. *Noise voltage must not exist on the shield*; shield-to-conductor capacitance will couple the noise directly to the center conductor. *If shield currents are not returned properly, they can show up in a remote part of the system* and perhaps cause trouble in a location totally unrelated to the shielding problem that was "solved." ◘

Table 2. Applicability of shielding considerations

Consideration	Universal	Electric	Magnetic
Know the noise source, coupling medium, and receiver.	X	X	X
Different shielding techniques are required for different noise sources, coupling channels, and receivers.	X	X	X
In most situations, conventional circuit analysis using lumped elements can be used.	X	X	X
Connect the shield at the signal-source end only.		X	
Carry shields through connectors.		X	
Individual shields should not be tied together.		X	
Do not ground both ends of a shield.		X	
Do not allow shield current to flow, except for driven shields - to cancel magnetic fields		X	X
Do not allow voltage on a shield, except for guarding.		X	
Know *exactly* where noise current from the shield will flow.		X	
Use short connections to return noise current from the shield.		X	
Electrostatic shields have little effect in reducing noise resulting from magnetic fields.			X
Reduce magnetic fields by physical separation proper orientation, twisted pairs, and/or driven shields.			X
Know the receiver loop area and orientation to the field. Keep field at right angles and reduce the loop area by using paired conductors, preferably twisted pairs, and minimize wire lengths.			X
Use guarding in high-impedance circuits	X	X	
In high-impedance circuits, be extremely careful of shield noise	X	X	

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FAST, FLEXIBLE SWITCHED DUAL-INPUT OP AMP & COMPARATOR

Use This IC as a Modulator/Demodulator, Lock-In Amplifier, Phase Detector Synchronous Detector, Rectifier, Dual-Mode Circuit, ...And Much More

by Paul Brokaw, Moshe Gerstenhaber, and Steve Miller

Model AD630* is an unusual new low-cost, single-chip, precision analog IC that can be used for the above functions with little or no additional circuitry. As a lock-in amplifier, it can recover a 0.1 Hz sine wave, transmitted as a modulation on a 400-Hz carrier, from a band-limited, clipped white-noise signal approximately 100,000 times larger—a dynamic range greater than 100 dB.

FUNCTIONAL ARCHITECTURE

The stylized block diagram of Figure 1 shows the essential circuit elements of the AD630.[1] Despite the formidable appearance of its array of 20 terminals, which make possible a wide range of applications, the basic idea behind the AD630 is rather simple. It consists of a frequency-compensated op-amp output stage with two identical switched differential front ends (A and B), a differential comparator that controls the switching (CMP), and a set of jumper-programmable matched precision resistors—trimmed to produce closed-loop gain accuracies to ±0.05% and gain match (between channels) to ±0.03%.

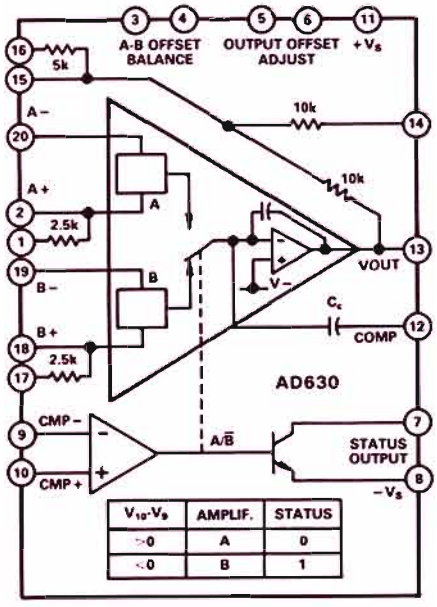


Figure 1. Functional diagram of the AD630.

When the input to the comparator's non-inverting input (CMP+) is more positive (or less negative) than the inverting input (CMP−), front-end A will be selected; when CMP+ is less positive than CMP−, B is selected. A status output, available via an open-collector transistor, indicates the comparator's state.

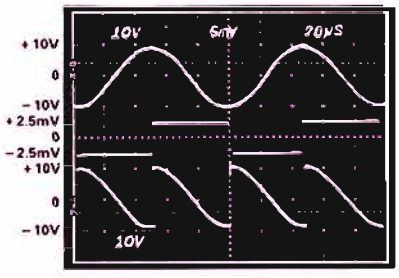
Suppose B is selected. The inputs labeled B+ and B− are the non-inverting and inverting inputs of an op amp, with output terminal at VOUT. It will behave just like an op amp with open-loop gain of 100 dB min, small-signal bandwidth of 2 MHz, and slew rate of 35 V/μs, and will perform the many functions op amps are used for. Offset voltage is ±100μV max (AD630B), drift is 1 μV/°C typically, and input bias/offset currents are 100/10 nA. The precision resistors provided on-chip can be used for accurate inverting and non-inverting gains of −1, −2, −3, and +1, +2, +3, and +4 V/V, without any external resistors. Other channel gains and op-amp circuits can be configured using external components.

Similarly, when A is selected, the device will behave like an op amp, with non-inverting input at A+, inverting input at A−, output at VOUT, and the same specs as for B. The same set of resistors can be used for circuits involving both A and B, because the unengaged front end's impedance remains high when it is deselected.

This flexibility permits the device to function in a wide variety of applications. It can produce dual-mode operation with differing magnitudes and polarities of gain for a single input, or it can multiplex two inputs with differing gains and polarities. Because the comparator can be driven by either a digital signal or an analog signal of sufficient magnitude, the device can also be used recursively, with the output affecting the state of the comparator.

HOW IT IS USED

The device may be used as a phase-sensitive detector with gain of 2, for a modulated signal voltage, by comparing the signal's phase with that of a control voltage at the same frequency as the carrier. When the control voltage ($V_{CMP+} - V_{CMP-}$) is positive, the gain is positive, and when the control voltage is negative, the gain is negative. Thus, the output will be positive when the signal is in phase with the control voltage, negative when the signal is 180° out of phase, and zero-average when the signals are in quadrature (Figure 2).



b. QUADRATURE DETECTION
UPPER - SIGNAL INPUT
CENTER - PHASE INPUT
LOWER - SIGNAL OUTPUT

Figure 2. Waveforms at quadrature in a synchronous detector.

Figure 3 shows a scheme for operation in this mode. When the control voltage, applied to the comparator, is positive, Channel A is selected; for negative control voltage, Channel B is selected. Channel A has a gain of +2, and Channel B has a gain of −2.

As Figure 3 shows, the input is applied to the non-inverting input of A, via the internal 2.5kΩ bias-current-compensation resistor, at pin 1, and also to the inverting input of B, via a 5-kΩ input resistor, at pin 16. The inverting inputs of A and B are connected together, and to the tap of the 10-kΩ feedback divider, but only one front end is working at any given time.

*Use the reply card for technical data and applications information.

[1]See 1982 IEEE International Solid-State Circuits Conference *Digest of Technical Papers*, p.44.

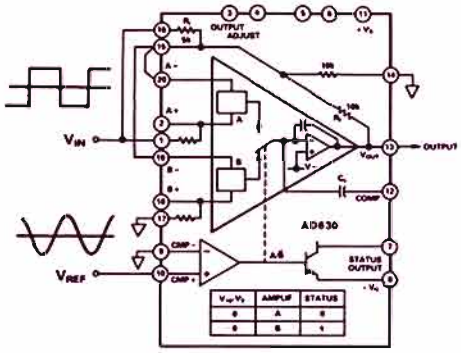


Figure 3. AD630 applied as a synchronous detector.

To understand how it works, we will consider ideal cases; actual operation is not greatly dissimilar. When A is selected, the feedback to A− must be almost exactly equal to the voltage at A+. In the ideal case, no current flows to B−, no current flows in the 5-kΩ resistor (since $V_{A-} = V_{IN}$), and no current flows to A−; therefore $V_{A-} = V_{OUT}/2$, hence $V_{OUT} = 2V_{A-}$.

When B is selected, the device looks like an inverting op amp, programmed for a gain of −2, with $R_i = 5$ kΩ, $R_f = 10$ kΩ, and a 10-kΩ load to ground at the summing point: $R_f/R_i = 10$ kΩ/5 kΩ. Since the voltages at both ends of the grounded resistor are zero, no current flows, and its loading effect is negligible.

Although A− and B− are connected together, there is little or no interaction, since both front ends are always at high impedance, even when they are disengaged from the device's output stage. However, the load seen by the *external* input (V_{IN}) can change (for example, in this case, it is 5kΩ when B is selected and at very high impedance for A); therefore, the signal driving point should be at low dynamic impedance, to avoid intermodulation effects.

The device is housed in a 20-pin DIP, and it has a supply voltage range of ±16.5V to ±5V, with 4-mA typical quiescent current drain. With ± 15-volt supplies, its input common-mode range is ± 10V (CMR = 90 dB min – B version), and the specified minimum output range is ± 10V into a 2-kΩ load; power-supply rejection is 90 dB min. Settling time is 3μs to 0.01% for a 20-volt step, and channel separation at 10 kHz is 100 dB. It is available in two −25°C-to-+85°C grades (AD630A and AD630B), differentiated principally by offset, drift, gain error and mismatch, and the AD630S for −55°C to +125°C. Prices (100s) are $9.95/$14.95/$18.95 for A/B/S.

APPLICATIONS

The AD630 was intended for wideband, low-level, and wide dynamic-range instrumentation applications. It is capable of such analog signal-processing functions as balanced modulator, balanced demodulator, absolute-value amplifier, phase detector, square-wave multiplier, and two-channel precision multiplexer.

Figure 4 is the schematic diagram of a circuit to demonstrate the dynamic range of an AD630 as it might be used in a lock-in amplifier. Lock-in techniques are frequently used to separate a small narrow-band signal from interfering noise. The lock-in amplifier serves as both narrow-band filter and detector.[2] When the frequency and phase of the signal are known, very small signals

[2]See "Lock-In Amplifier Uses Single IC," *Analog Dialogue* 8-1 (1974), for an example of a lock-in amplifier employing a differential instrumentation amplifier and external active and passive components.

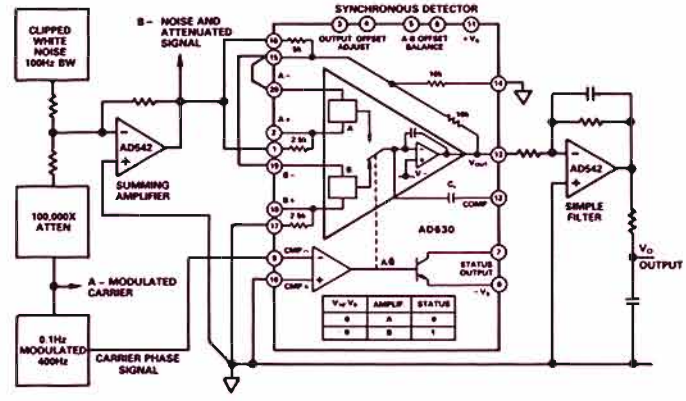


Figure 4. Lock-in amplifier circuit.

can be detected in the presence of large amounts of uncorrelated noise.

The lock-in amplifier is basically a synchronous demodulator, followed by a low-pass filter. An important measure of performance is the dynamic range of its demodulator. Figure 5 shows the recovery of a signal modulated at 400 Hz from a noise signal approximately 100,000 times larger, a dynamic range of 100dB.

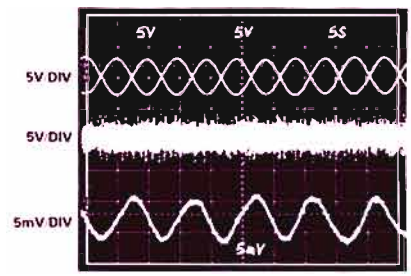


Figure 5. Waveforms for lock-in amplifier (see text).

The test signal is produced by modulating a 400-Hz carrier with a 0.1-Hz sine wave. The signals that are produced by chopped radiation detectors (infra-red, optical, etc.) may have similar components; a sine wave is used for clarity of illustration. This signal, present at point "A" of Figure 4, is shown by the upper trace of Figure 5. It is attenuated 100,000 times, normalized to the output "B" of the summing amplifier. A band-limited clipped white-noise signal, which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. Figure 5's center trace shows the sum of signal and noise at point B.

The combined signal is demodulated synchronously, using phase information derived from the modulator, and the result is low-pass filtered using a simple 2-pole filter with a dc scaling gain of 100. This recovered signal is the lowest trace of Figure 5.

The combined signal contrived for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100 dB of signal range, and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than that used in this example. A more-sophisticated low-pass filter will aid in rejecting wider-bandwidth interference.

Incidentally, an AD630 was also used as the modulator for the circuit of Figure 4. These examples illustrate the power of the AD630 in just one of its applications. A general-purpose device, its many latent uses challenge the creativity of the potential user. ◘

LEVEL-INDEPENDENT AUTOMATIC GAIN CONTROL

LOGDAC™ Controls Output Signal Amplitude Over Wide Range of Input
AD7111 Resolves to 0.375 dB, Provides Digital Readout of Input Level

by John Wynne

Figure 1 shows the essential components of a basic automatic gain-control (AGC) loop: the dc reference signal, V_{REF}, establishes the output amplitude set-point; the output-measurement circuit obtains a running measure of the output level, based on a property (peak, average, rms, etc.) of the output signal; a comparator, derives a control signal; and a gain-adjustment circuit, applies enough distortionless gain or attenuation to the input signal to maintain the output level sufficiently close to the reference value.

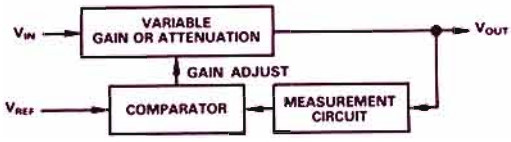


Figure 1. Automatic-gain-control loop.

The circuit examples shown here were designed to control output amplitudes for more than 40 dB of input range, for signal frequencies to beyond 20 kHz. Two cases are shown: in one, the input signal arrives at a higher level than the required output and must be attenuated; in the other, a low-level signal requires gain.

AGC WITH LOGDACS

The LOGDAC™ is a class of multiplying digital-to-analog converter that accepts bipolar analog input signals and provides an exponential (antilog) relationship between the digital input and the analog gain (or attenuation). For example, the AD7111* has an 8-bit µP-compatible digital input, with resolution of 0.375 dB per bit and a dynamic range of up to 88.5 dB of attenuation.

Among their many applications, logarithmic DACs are useful in automatic level control applications employing multiplying DACs. The salient features that make them desirable include their wide dynamic range and their equal-percentage-per-bit gain change. For example, when the input code of a *linear* 8-bit DAC changes by 1 bit near full scale, the fractional gain change is of the order of 1/250, and when the code changes by 1 bit near zero, the percentage gain change is of the order of 100%; on the other hand, the nominal gain change of an AD7111 over the active range of digital input is a fixed 0.375 dB—or 4.4% of reading—per bit.

In Figure 2, an AD7111 controls the attenuation for applications in which the input is at a high level compared to the output. With op amp A1, the regulator output amplifier, the AD7111 produces whatever attenuation of the analog signal input is required to maintain the output level. The digital input is increased or decreased, one 0.375-dB step at a time, by an 8-bit up/down counter. The counter, pulsed by a clock, is driven in the appropriate direction by the output of a comparator, A6, which compares the reference voltage with an amplified (A2), peak-rectified (A3) version† of the measured output voltage. The window comparator, A4 & A5, provides hysteresis, so that counting is inhibited when the output level is within a defined range of values.

*Use the reply card for technical data.

†RMS could also be employed, with excellent results, using the AD636 RMS-to-DC Converter.

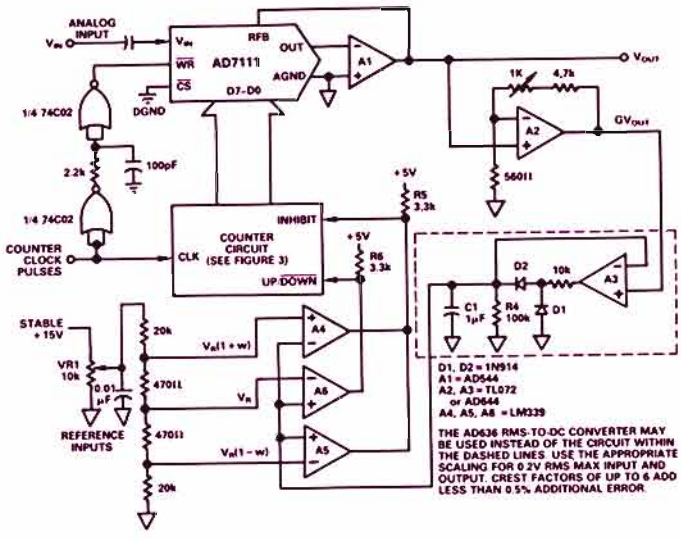


Figure 2. AGC loop using AD7111 for attenuation.

For the application shown here, the nominal output level is about 100 mV peak-to-peak. A2 provides amplification of the signal, about 10X, before it is peak-rectified. The reason for amplification is that the ripple content of the peak-detector output is not a constant percentage of signal amplitude—lower signal levels are accompanied by higher percentage ripple, which can lead to poor regulation when the input to the rectifier is well below 0.5V peak. V_{REF} should be scaled by the same amount as the closed-loop gain of A2. Thus, if A2's closed-loop gain is 10, V_{REF} should be 0.5V for a 50-mV peak output level. The input should be either ac-coupled, as shown, or symmetric about zero, to avoid the possibility of an input bias driving the peak-follower negative.

The output of the peak follower is compared with V_{REF} in A6, and with $V_{REF}(1 + W)$ and $V_{REF}(1 - W)$ in A4 and A5. The counter (Figure 3) will count down if the rectified voltage is less than V_{REF}, decreasing the AD7111's attenuation—and up if greater, to increase attenuation. If the rectified voltage is within about ± W of

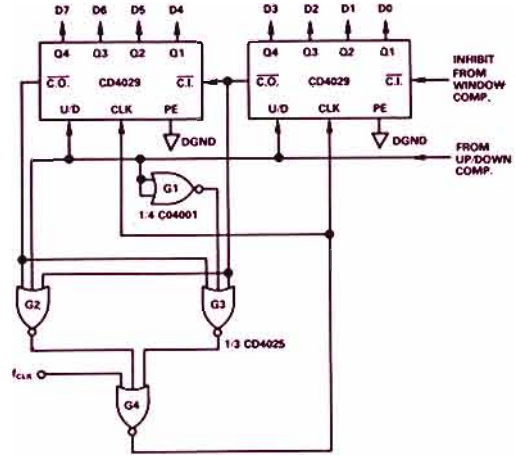


Figure 3. Counter circuit for Figures 1 and 4.

V_{REF}, the count will be inhibited, in order to provide sufficient hysteresis to avoid a ± 1-bit high-frequency "hunting" of the amplitude. In this example, W is about 2.3%.

Figure 4 is a plot of response at selected frequencies from 100 Hz to 20 kHz for a sine wave input from 0 dB to +40 dB, relative to the output level, which corresponds to 100 mV peak-to-peak. Note the flat response over the whole range of amplitudes. There is some variation with frequency (not a problem at fixed carrier frequencies) due to the rectifier's dynamic response characteristics.

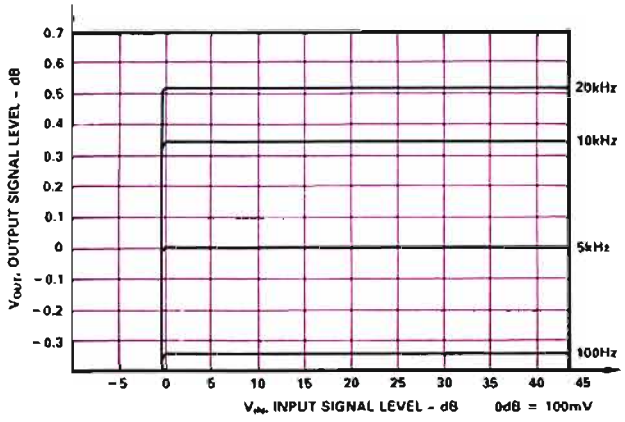


Figure 4. Response characteristics of circuit of Figure 2.

Figure 5 shows the corresponding circuit employed for applications in which the input is low and must be amplified to reach the desired output level. The AD7111 is connected to attenuate the feedback around A1, thus providing overall gain. An increasing digital input to the AD7111 will cause the feedback attenuation to increase, thus increasing the overall gain in 0.375-dB-per-bit steps. Since the output level is sufficiently high for good results with the peak detector, the scaling amplifier (A2 in Figure 1) is omitted. Thus, for 6.5 volts peak-to-peak, V_{REF} is 3.25 V.

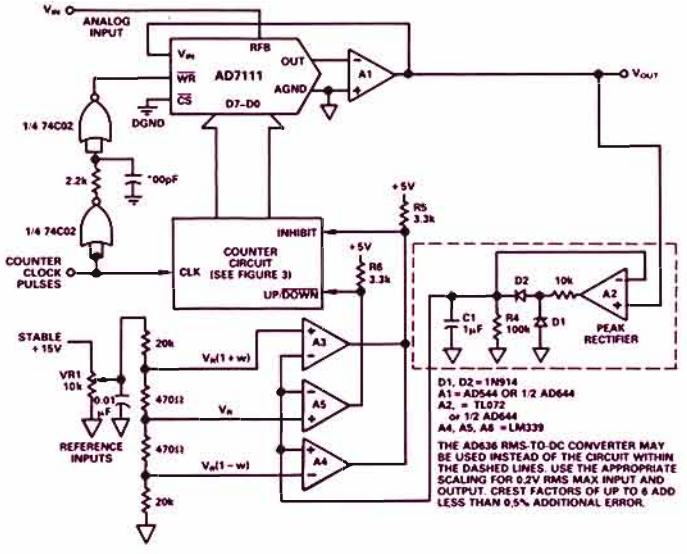


Figure 5. AGC loop using AD7111 for gain.

The response of this circuit, for an input sine wave of amplitude from 0 to −40 dB, referred to the output, is similar to that shown in Figure 4. Figure 6 shows the transient response of the circuit of Figure 5 to + and − 6-dB steps (50% amplitude changes) of a 1-kHz input signal. Settling occurs within about 130 milliseconds, using a 125-Hz clock frequency for the counter circuit. (At 125 Hz, the pulse period is 8 ms, and at 0.375 dB per step, 16 steps are required to reach 6 dB. The count stops when the *inhibit* band is reached.)

The response of the system is determined by the relation between the frequency of the clock used for the up/down counter and the lowest expected fundamental signal frequency. The lower that signal frequency, the longer the filter discharge time-constant must be, in order for the ripple to be kept within the comparator window between signal peaks. Then, if the clock frequency is too high, a step increase in the signal level will result in an undershoot of the regulated response. The reason? Although the output responds immediately to the input and the gain control, the peak-follower output that is fed back responds quickly to increases but decays slowly on decreases—one or more additional clock cycles may occur before the reference level is reached, temporarily allowing the actual amplitude to be brought below its final value. A useful rule of thumb: establish a clock frequency from 1× to 2× the lowest signal frequency.

If the input can be both larger and smaller than the output, the regulating circuit must be able to provide both amplification and attenuation. This is achieved by increasing the gain of A2 in Figure 1 by an amount equal to the lowest value of the minimum signal level (in dB, referred to the output). For example, if the input signal is expected to swing from −10 dB to +20 dB, referred to the output, then the gain of A2 should be increased by 10 dB to insure that the AGC loop is active over the entire input signal swing.

A/D CONVERSION

While performing their AGC function, these circuits also act as tracking analog-to-digital converters, since the varying digital code present at the counter output (AD7111 input) represents a logarithmic measure of the ratio between the analog input and output levels (i.e., the attenuation or gain required for correction). This output may be used for any digital purpose (storage, computation, etc.) or for driving slaved AD7111s to set gains elsewhere in the system in proportion to changes in the analog input.

Since the AD7111 has on-chip registers, the digital code can be latched, freezing the gain of the system. This can be vital in applications where the input signal may disappear altogether, e.g., due to excessive fading or an interruption in the signal path. In many AGC systems, when this happens, the gain of the loop will increase to maximum, which can result in system oscillation when the input signal is restored. The digital control word (Figure 1 or Figure 4) can be frozen by bringing $\overline{CS}$ (Chip Select) high. In such applications, $\overline{CS}$ can be driven by a suitable input signal detector, set to detect out-of-range input signals.

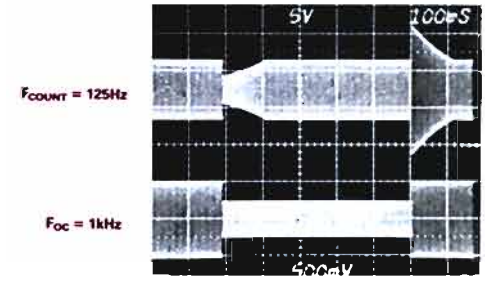


Figure 6. Response of circuit of Figure 5 to ±6-dB input changes.

12-BIT, 10-MHz ANALOG-TO-DIGITAL CONVERTER

Model CAV-1210: Complete on a Card – No External Components
Use It in Oscilloscopes, RADAR, Imaging Systems, Real-Time Spectrum Analysis

by Jerry Neal

The CAV-1210* is a complete 12-bit, 10-MHz A/D Converter on a printed-circuit card, introduced recently by the Computer Labs Division of Analog Devices. Complementing an extensive line of high-resolution, high-speed ADCs, the CAV-1210 includes a track-and-hold amplifier, an encoder, timing, and output registers. With it, you eliminate the costly in-house design effort associated with turning monolithic encoders into functioning a/d converters.

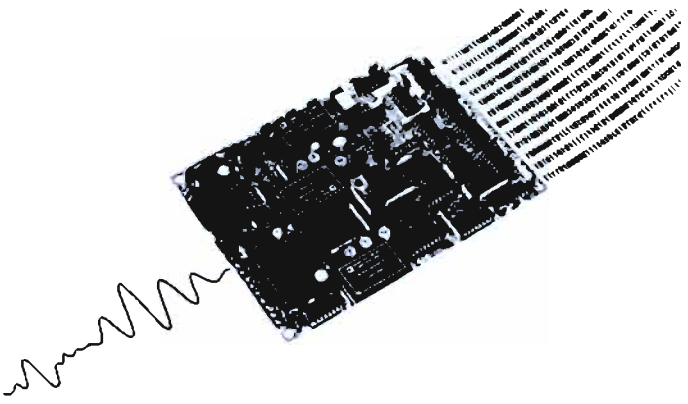
Because of its completeness, as well as its high resolution and conversion rate, the CAV-1210 can easily be integrated into a variety of system applications involving high-speed data acquisition and signal processing. Examples include medical imaging, digital oscilloscopes, radar digitizing, signature analysis, digital communications, and real-time spectrum analysis.

Like its predecessors, the CAV-1210 is a complete converter; it has internal track-and-hold, timing, encoding—employing digitally corrected subranging—output registers, and all of the necessary circuits to perform the conversion function without external components. The user supplies only industry-standard power levels (±15V, −5.2V, and +5V) and an Encode Command signal, which establishes the update rate of the output data. Monotonic performance is guaranteed over the entire 0°C to +70°C operating temperature range. Unit price is $3,165 in small quantity, with substantial volume discounts available.

Table 1 provides a comparative summary of available ADI card-level video converters. The ECL devices, in particular, have many features in common, including their basic design architecture, output logic structure (both true and complementary outputs are available), and similarity of pinout for various input and output functions. The only difference is in the extra pins for the additional output bits.

This pin-compatibility among the ECL-compatible products enhances their usefulness in systems that are designed for upgradable input dynamic range (bits of resolution) without requiring major modifications to system architecture.

Important specifications include *ac linearity* (defined in terms of spurious in-band signals generated at given input signal frequencies with a 10-MHz encoding rate)—spurious signals are typically 70 dB below full scale for dc to 1 MHz and −65 dB for 1 MHz to 5 MHz; *two-tone linearity*(defined in terms of spurious in-band signals generated by two nearby signal frequencies)—typically −70 dB for 60 kHz and 62 kHz, −65 dB for 2.498 and 2.500 MHz, and −60 dB for 4.996 and 4.998 MHz. With a 500-kHz analog signal, *signal-to-noise ratio* (rms) is 62 dB and *noise-power ratio* is guaranteed at 52 dB, minimum.



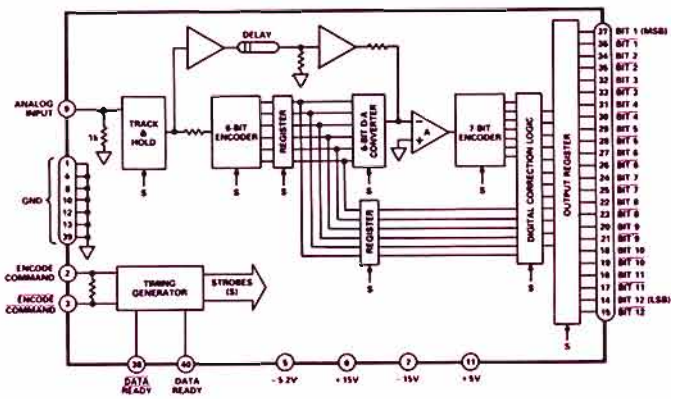


Table 1. Card-Level Video Converters from Analog Devices

Model Number	Resolution	Word Rate	Logic Family	Temperature Range
CAV-0920	9 Bits	20 MHz	ECL	0°C to +70°C
MOD-1005	10 Bits	5 MHz	TTL	0°C to +70°C
MOD-1020	10 Bits	20 MHz	ECL	0°C to +70°C
MOD-1205	12 Bits	5 MHz	TTL	0°C to +70°C
MOD-1205MB	12 Bits	5 MHz	TTL	0°C to +70°C
CAV-1210	12 Bits	10 MHz	ECL	0°C to +70°C

APPLICATIONS

The salient advantage of the CAV-1210—its combination of high speed and high resolution—make it useful wherever large amounts of data with wide dynamic range must be handled. Here are a few possibilities:

Among its most important applications areas is radar systems, which require wider dynamic ranges in order to increase their ability to distinguish targets in high-noise environments. Since wide dynamic range for search radars translates into more bits of converter resolution, the 12-bit CAV-1210 is highly appropriate for radars which must operate in high-clutter conditions. Similarly, it is useful in related applications, such as electronic countermeasures (ECM) and ECM test systems, which also require wider dynamic ranges.

tions are the possibilities in lab applications and in the whole spectrum of emerging applications for digital signal processing, discussed earlier in this issue— for example, digital oscilloscopes and digital radiography. In such applications, the better the quality and speed of the input data, the greater the possibilities for obtaining accurate results in real time. ◘

*Use the reply card for technical data.

MODULAR ALARM LIMIT SUBSYSTEM IS VERSATILE & RUGGED

4B Series Has High and Low Alarms, LED, Relay, & TTL-Compatible Indication Accepts High-Level Voltage, Process Current, or Outputs from 3B Subsystems

by Dave Reynolds

The 4B Series Alarm Limit Subsystem*, a rack-compatible system of plug-in modules that provide adjustable alarm limits for a variety of process sensors and transducers, was designed to handle the need for rugged, modular, accurate, versatile alarms at low cost.

Alarm units accept signals from process or other sensors, make decisions, and produce output indications for alarm or on-off control when monitored conditions fall outside specified limits. Typical applications include process control, factory automation, energy management, and data acquisition and control.

The Alarm Limit Subsystem accepts high-level voltage or current-loop signals, and provides fully independent HI and LO relay outputs, TTL outputs, LED indication, and (optionally) 3-digit readout. Although it can stand alone, it has been designed to work in conjunction with the 3B Series Signal Conditioning Subsystem* (introduced in *Analog Dialogue* 16-3), which interfaces directly to a variety of process sensors and transducers and transforms the inputs to standardized high-level analog outputs.

The 4B Subsystem consists of a 19"-relay-rack-compatible universal mounting backplane and a family of plug-in alarm limit modules (up to 12 per rack). A four-channel backplane, also available, handles simpler requirements at lower cost per channel. The modules, designed for voltage or current inputs, can be mixed and matched and are interchangeable without disturbing field wiring. Each backplane incorporates screw terminals for field-wired inputs and a connector for high-level single-ended inputs from 3B or other user equipment. Figure 1 is a photograph showing the salient elements of the system.

Each alarm module accepts a standardized high-level analog input and has two set points; both are adjustable to any value up to 100% of input span to provide one or two ON/OFF outputs. The 3 available input-range options are 0 to +10V/±10 V, 4-20mA, and 0-20mA.

The two set points within each module can be user-configured with push-on jumpers for HI-LO, HI-HI, or LO-LO use. If only one limit per channel is desired, the module can be used in a HI or LO state. The value of each set point and of the process variable can be viewed with a 3-digit display, controlled by a rotary switch.

Figure 2 is a functional diagram of the Model 4B10 voltage-input alarm limit module, configured for HI-LO operation. The input is filtered and compared with the HI and LO set points. If the process variable > HI or < LO, the appropriate relay is turned on.

Each set point has an adjustable deadband (0.5% – 10.0% of span); it establishes the minimum signal change necessary, after an alarm has occurred, to restore the unalarmed condition, to eliminate annoying reversals. For example, if HI is set at 75% of span, with 2% deadband, the alarm will turn on when the process variable reaches 75% but will not turn off until it drops below 73%. For a LO limit configuration, the deadband relationship is reversed; the the process variable must rise appropriately to turn off the alarm.

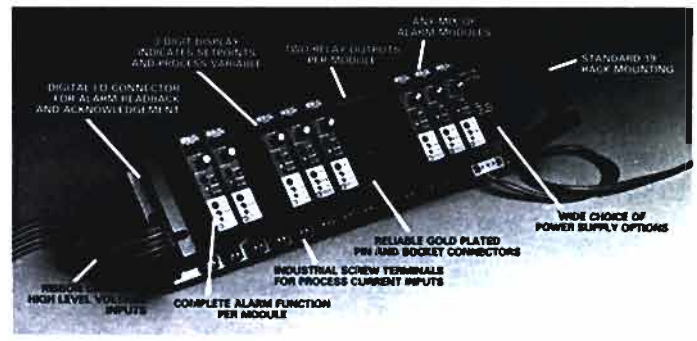


Figure 1. 4B Alarm Limit Subsystem is modular and easy to use.

An LED provides visual indication for each setpoint when an alarm condition occurs. The alarm status of both limits can be monitored externally ("readback") via the digital I/O connector, which also provides for external control or alarm acknowledgment ("override"). When an alarm state exists (TTL high), the relay can be turned off by an external signal (TTL low) on the "override" pins; the readback signal continues to remain high until the process variable itself is outside the alarm range.

APPLICATIONS

Key strengths of the 4B Series, applied to measurement and control, are ease of use and flexibility. In a typical application with the 3B Series Signal Conditioning Subsystem, the 3B modules interface directly to the sensors and produce two simultaneous high-level outputs (0 to +10V and 4-20mA), one of which (e.g., the voltage signal) could provide local alarming via the 4B Series, while the other (viz., the process current) could be used for remote transmission of data to the host computer. The alarm-indication function is sensor-independent; the appropriate 3B module does the signal conditioning. Besides being compatible with 3B Signal Conditioning Subsystems, the 4B Series provides alarm indication and on-off control when used with field transmitters or any other devices that provide process current or high-level voltage output.

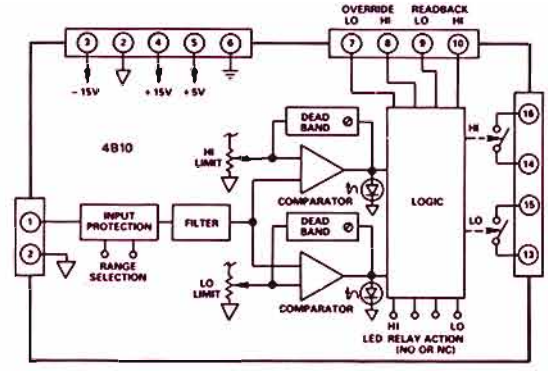


Figure 2. 4B10 voltage-input alarm module.

* For technical data, use the reply card.

TEST DIGITAL AND LINEAR ICs WITH LTS-2000 TEST SYSTEMS

LTS-2500 Family Board Adds Digital Test Capability to ADI Benchtop Testers

Test MOS and Bipolar SSI & MSI Logic Devices with up to 24 Digital Pins

by David Laing

At one stroke, the LTS-2500* Digital Device Family Board has added a new dimension to LTS-2000 Series Test Systems, extending their test capabilities to TTL and CMOS devices, as well as the standard repertoire of ADCs, DACs, and linears (e.g., op amps, comparators, timers, and regulators). As the first benchtop test systems able to test both linear and digital devices, the LTS-2000, LTS-2010, LTS-2012, and LTS-2015 now save time and effort for the many users who must test both types of device—by providing a common mainframe, software, and system philosophy, plus a nominal increment of dedicated hardware and software.

TEST DEVICES WITH UP TO 24 PINS

For testing digital devices with up to 24 active pins, The LTS-2500 package includes the family board, with a programmable 4-quadrant V/I source, 24 software-programmable driver/detectors, interactive debugger software, and a CREATE software package. A socket assembly and six different DUT (device under test) boards (with 14, 16, 18, 20, 22, and 24-pin sockets) are available for interfacing specific devices with the family board; the DUT boards are prewired with ground and a programmable 0-20V V_{CC} supply at the standard pin locations, and all pins are link-programmable. Figure 1 shows the principal elements of the LTS-2500 and its accessories. Testing both SSI and MSI (Small-Scale and Medium-Scale Integrated) logic devices with up to 24 digital pins, the LTS-2500 handles both MOS and bipolar technologies, including RTL, DTL, TTL, I^2L, MOS, CMOS, and NMOS. Each device pin is programmed in software, as to whether it is an input or an output, and is afterwards driven appropriately during tests.

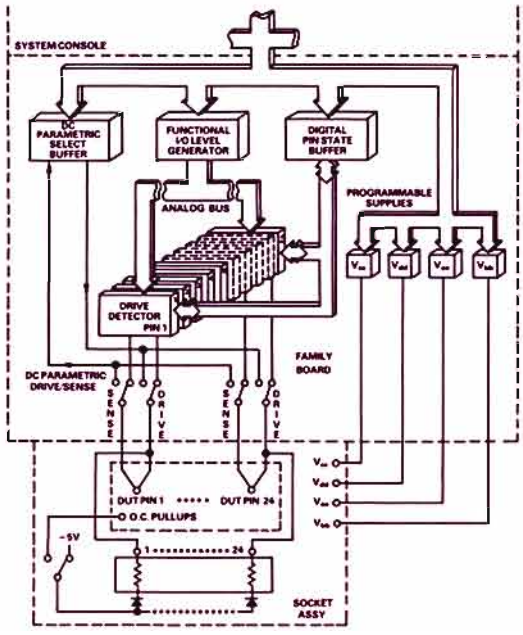
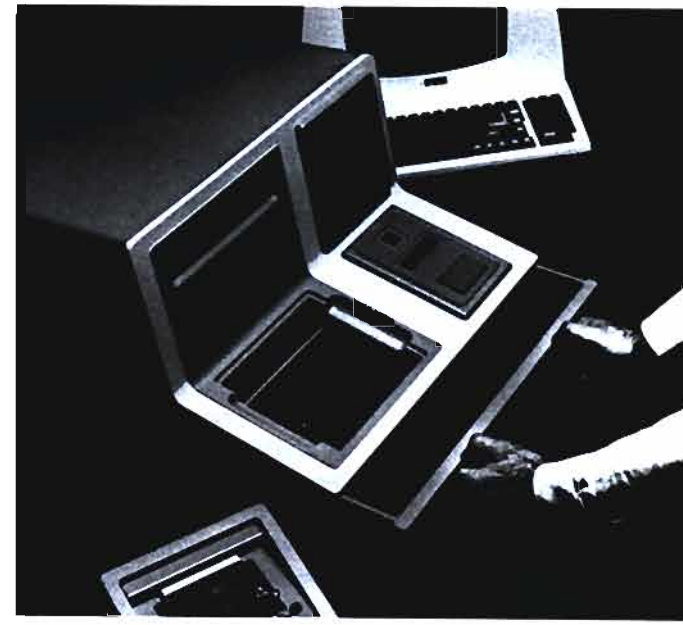


Figure 1. Functional block diagram of the LTS-2500 Digital Family Board.

*For technical data, use the reply card.



The system will test gates, counters, flip-flops, ALUs, and static RAMs, ROMs, and EPROMs. In addition, the LTS-2500 handles the full functional testing of analog switches. Testing is fast: for example, a test of 51 dc parameters of a 74LS95BN takes only 400 milliseconds, maximum. Multiple-level dc parametrics are automatically tested in a single pass.

The LTS-0650 Digital Device Socket Assembly, interfacing between the family board and the DUT socket board, has pullup resistors which are used in TTL logic test, when output pins are designated as open collectors. These resistors can be unplugged for testing CMOS, to ensure the required accuracy when measuring low currents. In addition to the accessories for standard devices, there's a General Purpose Application Socket Assembly—the LTS-0605—and General Purpose Application DUT Board—the LTS-0325, which can be user-configured for custom applications.

FRIENDLY SOFTWARE

A unique feature of the user-friendly software accompanying the LTS-2500 is the spec-sheet format provided to users. When test programs are to be written for a specific device, you simply answer system-posed questions about the type of device. After the data has been entered in response to the questions, the system automatically looks up the device's test limits, based on the Texas Instruments Databook—for bipolar devices—or the Motorola Databook—for CMOS devices, and presents the limits on the CRT. You then need only to edit the test limits, if necessary (if not, no limits or test conditions need be entered).

Voltage-forcing and -measurement capabilities span ±20V, with 10-mV resolution and ±0.05% maximum error. Six ranges of current forcing span the overall capability of ±400 mA, with resolutions as fine as 10 nA and accuracies to within ±0.15%. Prices are: the LTS-2500, $5,000; the socket assembly, $700, and the DUT boards, $135 each.

CREATING A TEST PROGRAM

The flow chart in Figure 2 shows the elements of the Digital Create Test Editor program for the LTS-2500. Using it, we can show the easy step-by-step approach to creating a test program. After you've loaded the Program, the Main Menu will be displayed on the CRT.

Just type in the number of the function that you want. In this case, type in "1" to create a new test program. The system will then display a series of screens and your responses to the prompts displayed will define the device to be tested and the default conditions. For example, after you've selected the Create function above, the system will display a "New Device Definition" menu.

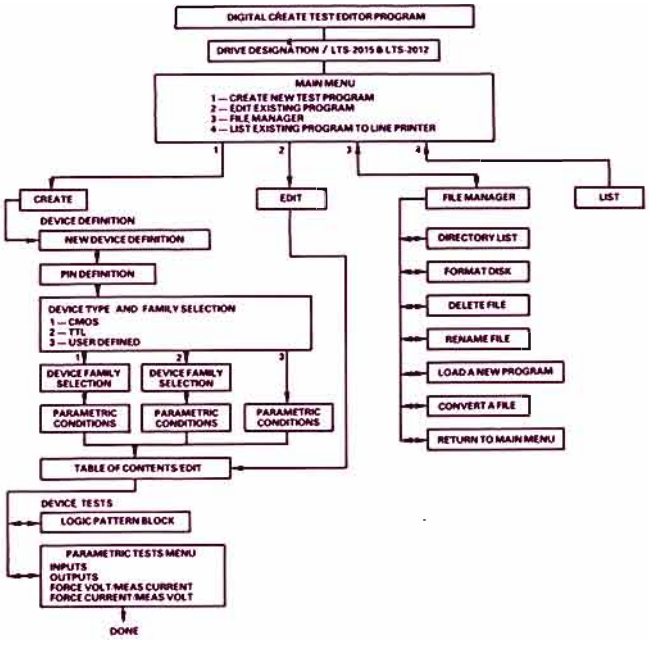


Figure 2. Digital Create Test Editor program.

Specifying the Device

You start with the DUT's file name, using up to 22 characters, then the number of logic pins (2 to 24) and the number of power/ground pins (2-5). If it is a multi-section device, enter Y for the next question; prompts will request the number of sections (2 to 8) and pins per section (2 to 8). When you've answered the prompts, the system will then display the appropriate Pin-Definition screen, depending on whether the device has one or more sections.

You enter into this screen the following information, taken directly from the device data sheet, for all pins except power and ground: the pin name, section (if multi-section), and function, i.e. input, output, open collector, etc. When all entries are made, a new screen appears, displaying the information you have entered, to verify the device pinout as it actually appears in the Data Book's device pin diagram (ALL OK? (Y/N)). If you find an error, you can return to the screen where it was made and correct it.

After the pin definition has been stored (Y), the Device Type Selection screen will appear, with three choices: 1. CMOS DEVICE, 2. TTL DEVICE, 3. USER-DEFINED DEVICE. Simply enter the number corresponding to the device to be tested, and the system will then display the Device Family Selection Screen with a list of logic families appropriate to your Device Type selection. For CMOS devices, the family selections include: Motorola CMS5, CMS10 and CMS15. For TTL devices, the family selections include: TI54XX, TI74XX, TI54HXX, TI74HXX, TI54LXX, TI74LXX, TI54LSXX, TI74LSXX, TI54SXX, TI74SXX.

Each of the selections for CMOS and TTL type devices provides default parameters based on the manufacturer's data sheets and the LTS system parameters. Just enter the number of your selection, and the default parametric conditions for that family will be displayed. You can change any or all of the values if you wish. (For the User-Defined Device screen, the parameter values, initially = 0, can be set to the desired values.) When you have responded affirmatively to the ALL OK? prompt, the device definition will be complete. The program next enters the Edit mode, in which you will specify the individual device tests for the test program. This mode can also be entered directly from the main menu.

Specifying the Tests

First, the Logical Pattern Block is established; it consists of a sequence of consistent states of all the logic pins with specified data and control inputs. For example, Figure 3 is an illustration of the first 7 steps of a 50-step Logical Pattern Block for a full-function test on an SN74LS193N 4-bit counter. The column headings, reading vertically, are CLEAR, DATA a through d, LOAD, CLOCKS (DOWN, UP), BORROW, CARRY, OUTPUT a through d; and the states shown are: H = high level, L = low level, \ = negative clock edge, and P = positive clock pulse. The last two designations, and the related / (positive edge) and N (negative pulse), for the clock inputs help to eliminate logic pattern programming errors on clocked devices.

Then the various tests are specified. Typically, full-function tests for the device are run at V_{cc}LOW and V_{cc}HIGH. In addition, TTL parametric tests to specified limits at one or more specified pins would include voltage measurements with forced currents (V_{ik}, V_{oh}, V_{ol} under 4 conditions) and current measurements with forced voltages (I_{ih}, I_{il}, and I_{os}).

The family board's *repertoire* of parametric tests includes 8 output (current and voltage) tests, 5 input (current and voltage) tests, and choice of Force Voltage/Measure Current and Force Current/Measure Voltage. Any number of tests, up to 47, can be run in any desired specified order. Default values are included wherever appropriate to speed up program creation. When all of the tests have been specified (and individually inspected), the entire test program with all of the tests included will be displayed. You may add, delete, or change tests. If there are no changes, write your program to disk and a return to the Main Menu screen will be executed.

The test software also has a real-time interactive Debug program, which stops at the first failure, or at a designated test, and allows you to examine and change the hardware/software setup—i.e., to do a fault analysis on a device during the actual test sequence. As Figure 2 indicates, all of the other functions of LTS-2000 series Create software are available in the LTS-2500 package.

	CLR	D a	D b	D c	D d	L D	D w n	U p	B r o	C r y	Q a	Q b	Q c	Q d
1	H	H	H	H	H	H	L	H	L	H	L	L	L	L
2	L	H	H	H	H	H	L	H	L	H	L	L	L	L
3	L	H	H	H	H	H	H	\	H	L	H	H	H	H
4	L	L	L	L	L	H	N	H	H	H	H	H	H	H
5	L	L	L	L	L	H	H	P	H	H	L	L	L	L
6	L	L	H	H	H	H	H	H	H	H	L	L	L	L
7	L	L	L	L	L	L	H	H	H	H	L	L	L	L
.														
.														
.														

Figure 3. Excerpt from a Logical Pattern Block.

UNDERSTANDING THE MACSYM 150/350 SOFTWARE

Operating Systems and High-Level Language: About MP/M-86® and MACBASIC 3
How an Unusual New Concept Combines Flexibility, Power, and Ease of Use

by Richard Quinn

In the last issue, we introduced the MACSYM 150/350 16-Bit Measurement-and-Control Computer System* and gave a brief overview of its hardware and software. Here we enlarge on a key factor in the system's flexibility, power, and usefulness—the MACBASIC 3 programming language and its companion software.

MACBASIC 3, like MACBASIC 2, is a version of BASIC that is expanded and optimized for real-time measurement and control. Special features included in MACBASIC 3 simplify input/output of analog data and digital control signals, while graphics commands let the user display and update graphic displays of measured variables in real time. Like its predecessor, MACBASIC 3 is *multitasking*—the user can write sections of the total process as independent tasks. System software automatically allocates hardware resources so that tasks run concurrently, with independent schedules and rates, rather than sequentially, as in single-task systems.

Instead of using MACSYM 2's proprietary operating system, dedicated to MACSYM 2 hardware, we decided to write MACBASIC 3 around a standard operating system, licensed from an outside vendor. The operating system had to: utilize 8086μP architecture; be real-time-interrupt driven; be multitasking; be disk-oriented; be recognizable by systems houses, OEM's, and end users; be flexible and easily adaptable to system upgrading; and be capable of running independently developed (third-party) software.

In view of these objectives, we considered the MP/M-86 operating system to be the single best choice for implementing a general-purpose real-time, multitasking measurement and control system for use in industrial laboratories and control rooms. So from the beginning, MACBASIC 3 was developed to utilize MP/M-86.

MP/M-86

Digital Research Corporation specializes in operating systems, program-development tools, and system-level programming languages for use on microprocessors. They created the *de facto* industry-standard operating system for 8-bit microcomputers, CP/M-80®. When Intel introduced the 8086, the first—and still the world's most widely used—16-bit μP, Digital Research responded by introducing an operating system for it, CP/M-86®. CP/M-86 has received worldwide acceptance and is supported by IBM, DEC, Wang, and other major computer manufacturers. As a result, a large body of third-party software has been written employing CP/M-86 as the standard operating system.

Because μPs with 16-bit architectures have the processing power to run more than one task at once, CP/M-86 spawned MP/M-86, which enables the 8086 to operate in multitasking real-time environments, formerly dominated by minicomputers.

*For a descriptive brochure on MACSYM 150/350 and a copy of the "MACSYM 150/350 Systems Digest," use the reply card.

®MP/M-86, CP/M-80, and CP/M-86 are registered trademarks of Digital Research Corporation.

ABOUT OPERATING SYSTEMS

An operating system is primarily a group of program modules which reside on the computer system and act as an interface between the application program, the user, and the actual hardware of the machine. Operating systems control such machine resources as the CPU, read-write memory (RAM), disk memory, keyboard, display, and peripherals, e.g., printers. High-level programming languages—MACBASIC 3, FORTRAN, Pascal—are not considered part of the OS; they use computer resources controlled by the operating system through standard operating-system calls. An OS allows a software developer to use sophisticated disk, display, and peripheral-control routines without concern for the programming of the associated hardware.

Multitasking operating systems have an added layer of responsibility. Examples of tasks are outputting to a printer, disk I/O, and floating-point numeric calculations. Single-task operating systems, like CP/M-86, can generally do only one thing at a time. Therefore, the CPU is idle most of the time during disk and printer I/O; this time is wasted. On the other hand, a multitasking operating system can concurrently handle all three tasks (and more, involving more I/O channels, memory, and most other computer resources); it uses the CPU for the floating point calculation, while also supervising the printer and disk I/O. A multitasking operating system must keep track of the exact state of all system priorities and allocate system resources to the most important tasks.

In addition to the conventional uses of multitasking to improve overall system performance, as described above, MACBASIC 3 goes further in the MACSYM 150/350, giving the user the capability of defining MP/M-86 tasks within the actual MACBASIC 3 program. For example, a user might wish to independently monitor and control ten different reactor vessels in a plant, check for alarm limits, and print one summary report on all ten vessels. With MACBASIC 3, the user can assign ten tasks for measurement and control, one task to check for alarm limits and one task to print the summary results. The CPU shares its time between the tasks, and they all appear to run at the same time. Priorities can be set so that control of the reactor vessels and alarm-limit checking have priority over printing.

MACBASIC 3

MACBASIC 3 is a high-level programming language designed for the applications-oriented measurement and control programmer. Its inherent features, such as specialized measurement and control commands, graphics commands, and multitasking, make it the ideal programming language for OEMs, systems houses, and sophisticated end users. The less-experienced programmer can learn it easily because it is basically BASIC. Figure 1 shows the relationship between software and hardware in MACSYM 350.

For MACSYM 150/350, the goal was to make the source code (i.e. the actual MACBASIC statements entered by the user from the keyboard) as compatible as possible with that of MACSYM 2, even though different computer hardware is used. The familiar

measurement and control commands, AIN, AOT, DIN, DOT, WAIT, TASK, etc., have the same function in MACBASIC 3 as in MACBASIC 2. Properly written MACBASIC 2 programs should run under MACBASIC 3 with little or no modification.

Using MACBASIC 3 for CRT graphics (a standard feature of the MACSYM 150/350), the programmer can define the world coordinate system of the graphics display using the WINDOW command. Up to four separate windows, each with its own coordinate system, can be displayed on the screen at once. Data can be plotted to the screen by using PLOT (vectors), BOX (rectangles), and CIRCLE commands. Plotting of X & Y axes is simplified with the use of HAXIS and VAXIS commands. Text can be printed to the screen using the HPRINT and VPRINT commands. The COLOR command sets the foreground and background colors. The same command language can also drive an optional 8-color plotter.

The user creates a program using the MACBASIC 3 screen editor. Since it is line-oriented, a user can change a line anywhere on the screen using dedicated editing keys, which include full cursor control, backspace, *insert* and *delete character*, *insert* and *delete line*, and tabbing. One line can be changed at a time, the change taking effect when the Return key is pressed. The MACBASIC 3 screen editor can save an enormous amount of time during program development, since the user does not have to retype entire lines which contain minor syntax errors.

As each line of source code is entered through the screen editor, it is analyzed and then compiled directly into machine code, line by line, by the MACBASIC 3 compiler, which automatically checks for syntax errors and notifies the user immediately. If a line compiles correctly, the original source code is placed in the source code module, while the resulting machine code is placed in the object code module. When lines are renumbered or deleted altogether, the changes are automatically entered into source code and recompiled into object code. This technique combines the ease of using interpreted languages like BASIC and the processing power of compiled languages like Pascal and FORTRAN.

Since the compiler runs as an MP/M-86 task, it can be "turned on" while a MACBASIC 3 program is running. A programmer or applications engineer can list out lines of source code, examine the state of key variables, change variables, and start and stop tasks while the program is running. Sophisticated control loops can be fine-tuned while the real-time effect of any changes is observed.

MACBASIC 3 makes extensive use of MP/M-86 structures known as resident system processes (RSPs)—tools and utilities which reside in RAM and on disk. The utilities accessed by a MACBASIC 3 program are all located in RAM, in order to insure the speed required by real time control. For MACSYM, new RSPs have been added to the operating system to optimize it for measurement and control. These RSPs include the screen manager (with graphics features) and the ADIO manager (with routines for accessing MACSYM 150's Series-100 I/O cards and the MACSYM 200 ADIO cards). RSPs also can also be used to add new features to MACBASIC 3 as the MACSYM 150/350 product line grows. Recently introduced RSP's include an 8-color plotter driver and a Series-100 IEEE-488 card driver. RSPs not needed for the user's final operating system can be deleted to conserve space in RAM.

A MACBASIC 3 program can contain from 1 to 18 tasks. MP/M-86 schedules which task gets control of the CPU and for how long. The highest-priority task will always run until completion or until

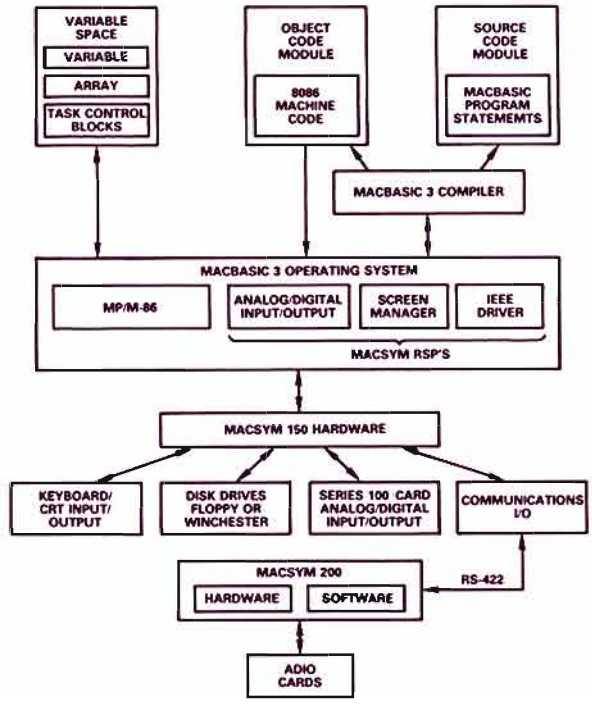


Figure 1. MACSYM 150/350 software/hardware architecture.

it is blocked (for I/O, WAIT, etc.). Equal-priority tasks time-share; each task executes for a fixed number of clock ticks before being put at the end of the execution queue. Tasks can be time-independent of each other, yet communicate through shared files and variables. Any task can start, suspend, or kill another task.

THIRD-PARTY SOFTWARE

Since MP/M-86 is a superset of the industry standard CP/M-86 operating system, properly written programs (which conform to standard CP/M-86 calls for use of system resources) should run under MP/M-86 with little or no modification. This means that much software written by other companies will run on ADI's MACSYM 150/350. Third-party software includes statistical packages, languages like Pascal and FORTRAN, and programs for word processing, electronic spreadsheets, asynchronous communications, and database management. Examples are:

WordStar – a highly effective word-processing program—the original draft of this article was written on a MACSYM 150 employing Wordstar; **SuperCalc** – a multipurpose 63 × 254 electronic spreadsheet for forecasting and planning; **dBase II** – a relational data-management tool to help users construct and manipulate numeric and character information files; **ABSTAT** – a statistical and data analysis package including regression, analysis of variance, skewness, kurtosis, t test, chi-squared test, and more.

At present, CP/M-86 programs must be adapted for MACSYM 150/350. The original manufacturer usually ships them on 8-inch floppy disks, which aren't compatible with 5 1/4" disk drives; or, if shipped on 5 1/4 inch disks, the programs are generally configured to work with a specific computer. To ensure availability of a wide variety of third party software for the MACSYM 150/350, a U.S. software distributor, Applications Unlimited, has entered into an agreement with us to configure and support third-party software on 5 1/4 inch disks for the MACSYM 150/350. Third-party software, ordered from this distributor, has been tested on a MACSYM 150/350 system to see that it works properly.

ULTRAFAST DAC

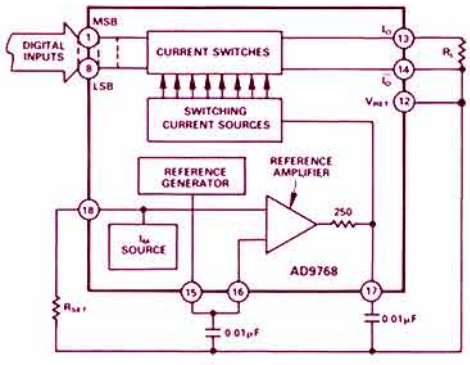
8-Bit Monolithic AD9768SD Settles in 5 ns

The AD9768SD* is a monolithic 8-bit digital to analog converter with typical settling time of 5 ns to 0.2%. It will operate either as a fixed-reference DAC, using its on-chip reference, or as a two-quadrant multiplying DAC with bandwidths to 40 MHz. Capable of 100-MHz update rates, it is ECL-compatible and provides a full-scale output current of 20 mA.

Its combination of high speed and low glitch impulse (200 mV-ns) suit it well for raster-scan and vector-graphic displays. The on-chip reference and associated amplifier reduce support-circuitry requirements for fixed-reference applications, while variable-reference signals at up to 40 MHz can be applied as either current or voltage of a single polarity for multiplying, modulating, and variable attenuation.

Its 20-mA current output can drive 50-ohm unbalanced or 100-ohm balanced transmission lines directly with 1-volt unipolar or ±1-volt amplitudes with a slewing rate of 400V/μs. Monotonic performance is guaranteed over the −30°C to +115°C operating (case) temperature range.

The AD9768's typical offset current is 60μA; its drift with temperature is 1.5 ppm/°C. Reference drift is 70 ppm/°C, output impedance is 830 ohms, and output compliance voltage range is from −0.7 V to +3.0 V. Specified to operate with +5 V and −5.2 V power supplies, the device is housed in an 18-pin hermetically sealed DIP and dissipates 430 mW max. Availability is from stock and the price is $32.20 in 100s.



*Use the reply card for technical data.

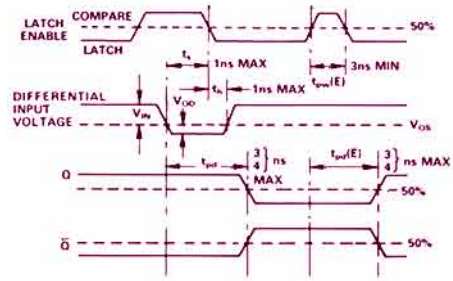
HIGH-SPEED SAMPLING COMPARATORS

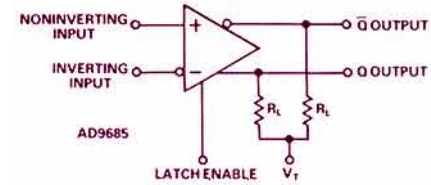
Monolithic Single AD9685 and Dual AD9687 Have Guaranteed Max 3 ns and 4 ns Propagation Delays

The AD9685* single and AD9687* dual sampling comparators, with guaranteed maximum propagation delays of 3 ns and 4 ns, and maximum latch setup time of 1 ns, are pin-compatible with the slower industry-standard 685/687 series.

Sampling comparators have a latch which, when enabled, holds the output state. Input changes will not affect the output until the latch has been disabled. The latches on the dual AD9687 can be separately enabled, for independently controllable comparators.

Sampling comparators are useful in analog and digital ATE applications, including high-speed window detectors, sense amplifiers, and peak-detector circuits. They





THE OUTPUTS ARE OPEN EMITTERS, REQUIRING EXTERNAL PULL-DOWN RESISTORS. THESE RESISTORS MAY BE IN THE RANGE OF 50Ω–200Ω CONNECTED TO −2.0V; OR 200Ω–2000Ω CONNECTED TO −5.2V.

can be used in settling-time test circuits for fast op amps and DACs, or with optical detectors to measure laser pulsewidths. Other applications include high-frequency VCOs, line receivers, track-and-hold amplifiers, threshold detectors, and ultrafast ADCs.

Both models have differential inputs with a ±2.5 volt input range and 80-dB CMR. Maximum offset is ±5 mV max, with drift of 20 μV/°C. The complementary (push-pull) outputs are ECL-compatible, operating from +5-V and −5.2-V power supplies. Both devices are available in 16-pin ceramic DIPs; the AD9685 is also available in a TO-100 can. All types are specified for operation from −30°C to +85°C. Pricing in 100s is $8.95/$15 for AD9685/AD9687.

VIDEO-SPEED OP AMP

HOS-060 Settles to 0.1% in 80 ns Has Output Range of ±100 mA at ±10 V

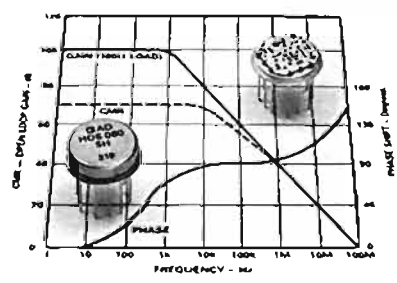
The HOS-060* video-speed op amp settles to 0.1% in 80 ns, features true-differential inputs and maximum initial offset voltage of ±1 mV, with drift of ±10 μV/°C. It will drive a load of ±100 mA to a minimum full-scale voltage of ±10 V.

Its high performance makes it suitable for high-speed applications such as fast settling d/a conversion, video pulse amplification, CRT deflection, wideband current boosting, and impedance matching. The 100-mA output current can drive coaxial cables directly. Its low output impedance and high input impedance permit it to buffer slow, accurate analog circuits from ADC inputs.

Rated performance is specified with ±15-volt power supplies over a −55°C to +125°C (case) temperature range. The HOS-060 works with supplies from ±12 V to ±18 V.

Open-loop gain (100-ohm load) is typically 100 dB, with CMR of 70 dB. Slewing rate is 300V/μs, input noise is 7μV rms (dc to 2 MHz), gain-bandwidth is 100 MHz, and overload recovery time is 400 ns. Maximum output impedance is 1 ohm.

The HOS-060SH and HOS-060SH/883 are housed in 12-pin hermetically sealed TO-8 packages. Prices (100s) are $105 and $185.

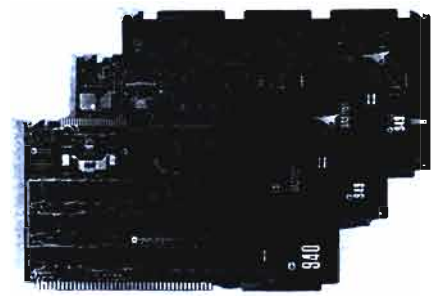


MULTIBUS-COMPATIBLE ANALOG I/O BOARDS

3 Boards Provide Input-only, Output-only, and Input/Output 16-, 20-, and 24-Bit Memory Addressing, 12-Bit Conversion

The RTI-711, RTI-724, and RTI-732* boards, direct replacements for industry-standard interfaces, provide analog input/output capability for MULTIBUS™-compatible microcomputers. Featuring jumper-selectable 16-, 20-, and 24-bit memory-mapped addressing and 12-bit resolution, these subsystems operate with all 8- and 16-bit MULTIBUS-compatible CPU boards, at processing rates up to 8 MHz.

The boards are designed to operate under Intel's RMX-80™ analog software drivers. Key features of the RTI-711 Input-only, RTI-732 Input/Output, and RTI-724 Output-only cards are summarized in the table. Input-board gains are software-programmable; the 4-to-20-mA outputs on output boards are optional to allow cost savings where they are not required. Sensors can be interfaced with via the 3B-Series Signal Conditioning Subsystem.



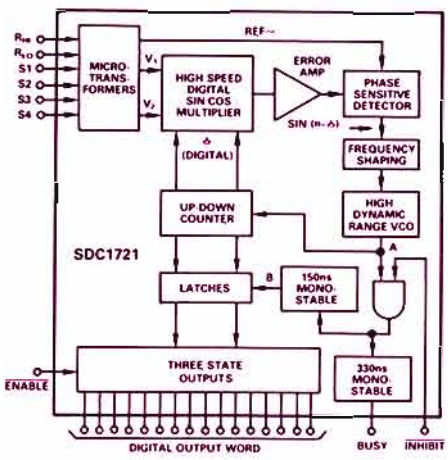
TM: Multibus and RMX-80 are trademarks of Intel Corp.

		INPUT BOARDS				OUTPUT BOARDS			
Model	Board Type	Channel Capacity Standard	Capacity Optional	Gain Range	A/D Resolution	Channel Capacity	D/A Resolution	4-20mA Output	Base Price (10-24)
RTI-711	Analog Input	16SE/8D	32SE/16D	1, 2, 4, 8	12 Bits	← N/A →			$580
RTI-732	Analog Input/Output	16SE/8D	32SE/16D	1, 2, 4, 8	12 Bits	2	12 Bits	2	$535
RTI-732-V	Analog Input/Output	16SE/8D	32SE/16D	1, 2, 4, 8	12 Bits	2	12 Bits	–	$445
RTI-724	Analog Output	← N/A →				4	12 Bits	4	$715
RTI-724-V	Analog Output	← N/A →				4	12 Bits	–	$670

16-BIT SYNCHRO-DIGITAL CONVERTERS

SDC1721/RDC1721 Have 3-States, Internal Transformers Continuous Tracking, Accuracy to ±40 Arc-Seconds

The SDC1721* is a 16-bit-output, high accuracy, continuous-tracking Synchro- or Resolver-to-Digital Converter with 3-state latched outputs. It employs a Type 2 servo loop, for zero steady-state position and velocity errors. Accuracy is to within ±40 seconds of arc (comparable to the angle subtended by a military tank at 100 km).



Use the SDC1721 to convert synchro or resolver signals to digital processor input in high-accuracy angle measurements. Typical application areas include test equipment, servomechanisms, antenna monitoring, simulation, artillery fire-control systems, and replacement of two-speed systems.

The input signals can be either 3-wire synchro (SDC1721) or 4-wire resolver (RDC1721), plus reference. Signal and reference frequencies from 360 Hz to 2.9 kHz may be used; the guaranteed minimum tracking rate is 3 revolutions per second. The digital output is TTL-compatible parallel natural binary, buffered by 3-state latches, simplifying multiplexing. It is housed in a 3.125″×2.625″×0.8″ module; prices start at $580 (1-9).

*Use the reply card for technical data.

18-BIT DAC

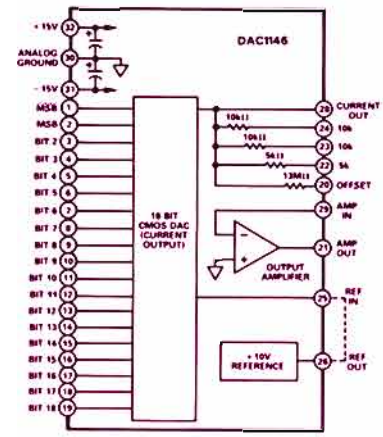
DAC1146 Has Low Cost Linearity to 0.00076%

Offering designers of high-precision instrumentation and digital audio equipment a cost-effective solution for generating precision voltages or currents, the DAC1146*, the industry's lowest-cost d/a converter having ±0.00076% full-scale accuracy and 18-bit resolution, is housed in a 2″×2″×0.4″ module. It is priced at $130 in 100s.

Functionally complete, the DAC1146 includes a precision output amplifier and a +10-volt internal reference. Analog output ranges of −2 mA, ±1 mA, +5 V, +10 V, ±5 V, and ±10 V can be selected by pin-jumper programming. Other output ranges can be obtained with an external reference.

The DAC1146 will operate with power supplies ranging from ±11.5 V to ±16.0 V, consuming 600 mW. The digital input coding can be binary, offset binary, or 2's complement. Its guaranteed maximum error specifications include differential and integral nonlinearity of ±0.00076% FSR (full-scale range), and tempcos of: differential nonlinearity, ±1 ppm/°C; offset, ±30μV/°C; gain, ±12 ppm/°C; and bipolar offset, ±7 ppm/°C.

The DAC1146 is also fully characterized for digital-audio applications. Audio parameters include 6-μs maximum guaranteed settling time to 0.00076% (full-scale step) and typical dynamic range of 96 and 100 dB for 16- and 18-bit inputs. Total harmonic distortion for a full-scale signal over the entire 20 Hz-to-20 kHz audio range is typically less than 0.002%, or −94 dB.



WORTH READING

The application notes, brochures, and reprints listed below are available from Analog Devices at no charge as long as the supply lasts. Software prices are as noted.

APPLICATION NOTES

"AD7528 Dual 8-Bit CMOS DAC Application Note," by Paul Toomey & Bill Hunt, 8 pages. Seven application areas are discussed, including programmable filter, oscillator, sine-wave synthesizer, voltage/current source, amplifier, waveform generator, single-supply applications.

"Using the ECL HDG Series in a TTL World," by Jim Haferd, 2 pages. Why ECL is used for HDG Display DACs; interfacing ECL devices to TTL circuits.

BROCHURES

Interfacing the Real World to Your Computer, 14 pages. Short-form catalog of modular signal conditioners & 2-wire transmitters (2B Series), signal-conditioning I/O subsystems (3B Series), μC-compatible analog I/O boards (RTI Series), complete low-cost measurement & control system for harsh industrial environments (μMAC-4000 Series).

Introducing the AD2050 and AD2051 Intelligent Thermocouple Meters, 4 pages. Description of μP-based thermocouple meters for J, K, T, E, R, S devices.

MACSYM Peripherals for MACSYM 10, 150, 350, 6 pages. CRT monitors, printers, touch-sensitive display terminals, plotters, disk drives, programming peripherals.

MACSYM 150/350 Systems Digest, 14 pages. Introduction to MACSYM 150/350 Measurement and Control Computer System hardware and software, with an example of multitasking, list of ADIO (analog/digital input/output) cards, summary of MACBASIC language, and specifications.

REPRINTS

"Automated Electrical Motor Testing Boosts Productivity," by Al Haun, *Assembly Engineering*, December, 1982, 4 pages. Describes use of MACSYM 2 in automated testing at Electric Motor Division of Gould, Inc.

"Design of Raster-Scan Graphics Systems," by Walter Kester, *Digital Design*, August 1982, 8 pages. Using HDG display DACs to design better displays.

"Test Video A/D Converters Under Dynamic Conditions," by Walter Kester, *EDN*, August 18, 1982, 10 pages. To characterize video-speed analog-to-digital converters adequately, comprehensive dynamic measurements must be made, with the data collected and properly evaluated.

SOFTWARE

LTS-0904 Linear Program Library Book, 350 pages.	$ 25
LTS-1600 Op-Amp Library on Disk	$475
LTS-1610 Voltage Regulator Library on Disk	$550
LTS-1620 Comparator Library on Disk	$125
LTS-1630 D/A Converter Library on Disk	$425

The *LTS-0904 Program Library Book* provides the user of Analog Devices LTS test systems with a complete CREATE menu for tests on each of over 300 linear devices, developed by Applications Engineers at our CTS division, using the LTS-2000, LTS-2010, LTS-2012, and LTS-2015 systems. Each device program, designed to operate on the factory-developed CREATE/TEST software, has been executed and is believed to be accurate and reliable.

The device programs are written to test those parameters guaranteed by the specified manufacturer; other manufacturers' devices may be tested without change, using the same program, but the reader is cautioned that components from different manufacturers with the same specifications may not react the same in a test circuit. Since properly configured test hardware is a must, wiring diagrams for the DUT boards are also included in the library.

As noted above, the programs are also offered in diskette form. The obvious advantage of the disks is that software development efforts are dramatically reduced, with only minimal limit changing if a different manufacturer's components have been specified for a given generic device. The LTS-0904 Program Library book is sent with each disk library ordered to provide full documentation.

Phone in your test-library order to (617) 273-4780, or mail it to:

Component Test Systems
Analog Devices, Inc.
10 Corporate Place
Burlington, MA 01803. ▶

MORE AUTHORS *(Continued from page 2)*

John Oxaal (page 3) is a Marketing Specialist on the staff of the Digital Signal Processing Division. Before joining Analog, he worked at the Duke University Medical Center, designing 2-dimensional ultrasonic imaging systems. John holds a B.S. in Biomedical Engineering from Duke and earned an M.B.A. from the University of Chicago.

Richard Quinn (page 22) is a Senior Marketing Engineer at ADI's Measurement and Control Systems Division. The author of "Powerful Measurement-and-Control System . . . and Much More," his biography and photograph appear in the last issue, 16-3.

Dave Reynolds (page 19) is a Senior Marketing Engineer for Systems Interface Products at Analog Devices. He authored the article, "Multichannel Signal-Conditioning Input/Output Subsystem," that appeared in the last issue, 16-3, where you may also find his biography and photograph.

Alan Rich (page 8) is a Staff Engineer—Product/Test Development at Analog Devices Semiconductor. He is author of a two-part series, of which the second part appears in this issue. The first part, entitled, "Understanding Interference-Type Noise," appears—with his biography and photograph—in the last issue (16-3).

John Wynne (page 16) is an Applications Engineer at Analog Devices, B.V. (Limerick, Ireland). Two articles by him appeared in a recent issue (16-2), "AD7528: A Dual Monolithic DAC for Many Reasons," and "Deglitching a 16-Bit Monolithic D/A Converter," along with his biography and a photograph.

Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

IN THE LAST ISSUE (Volume 16, Number 3, 1982 -- 28 pages):

Analog Signal-Conditioning ICs Take Two Giant Steps (Low-Noise Instrumentation Amp - AD524 and Thermocouple Preamp with Cold-Junction Compensation - AD594)
Multichannel Signal-Conditioning Input/Output Subsystem (3B Series)
Sensor-Based Intelligent Data Acquisition for the STD Bus (RTI-1270)
Powerful Measurement-And-Control SYsteM...And Much More (MACSYM 150/350)
Faster Testing with New Computer-Based Benchtop Tester (LTS-2015)
Industry's First Quad 12-Bit DAC in a 28-Pin DIP (AD390)
Understanding Interference Noise -- No Black Magic Required
Wideband Two-Channel Monolithic Analog Multiplier/Divider (AD539)
MACSYM Speaks; Introducing the SSP01 Speech Synthesizer Card
Highest Performance 12-Bit Monolithic D/A Converter Has Voltage Output (AD7240)
New-Product Briefs:
14/16-Bit Digital/Resolver Converters (Hybrid DRC1745/1746)
New DACs with Existing Second Sources (AD DAC71/72, AD3860)
IC Attenuator Has 0 to -19.9-dB Range in 0.1-dB Steps (AD7115)
Hybrid Track-Hold, 170-ns Acquisition Time to 0.1% (HTC-0300A)
9-Bit, 20-MHz Video A/D Converter with Track-Hold (CAV-0920)
8-Channel RTD Measurement Card for MACSYM (RTD01)
4-Channel Setpoint/Alarm Card for MACSYM (SPA01)
Isolated 4-to-20 mA or 0-to-20 mA Current Transmitter (2B23)
New Analog Devices Division Fellow Named: Mike Timko
Editor's Notes, Authors, New Literature, Potpourri, Advertisement

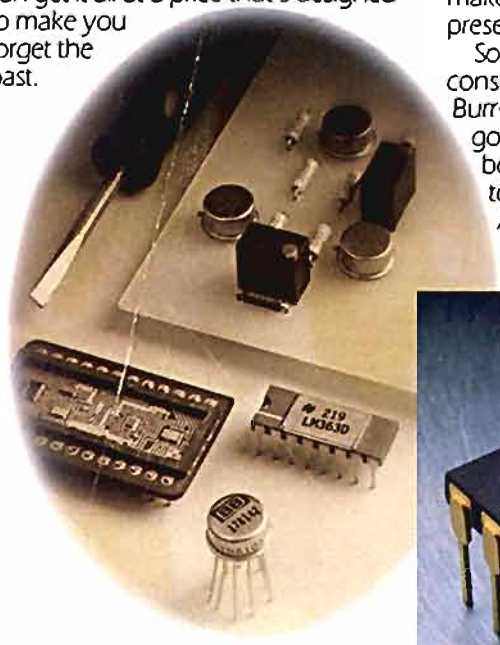
PRODUCT NOTES . . . AD566K/T and AD566AK/T - New full-scale gain-tempco spec: 2 ppm/°C typical, 5 ppm/°C maximum . . . Measured ADLH0033 input capacitance, using a +9-volt, 500-kHz, 50%-duty-cycle square wave: 2 pF. Same data for HOS-100: 9 pF . . . New specs for DTM1716/1717: Zero offset, 5 mV maximum; Analog input impedance 20,000 ohms; Power-supply quiescent current, max, 60 mA @ +15 V, 50 mA @ -15V . . . New specs for AD2712 and AD2702: Minimum Pin length, 0.190"; Supply current at -15V, -4 mA max . . . New specs for 2B54: Bias current, +8 nA max; Open thermocouple response not guaranteed without external bias resistor. . . . DRC1745/46: The STM1681 transformer, used with this device, now has separate grounds for the Sine and Cosine primary windings. They should be separately connected to the device's Signal Ground.

DATA-SHEET UPDATE . . . HTC-0300: Use the individual data sheet instead of the Databook, Volume I, data sheet for correct specification information, block diagram, and pin designations . . . CAV-1210: In the block diagram, page 3, the input at pin 9 has a fixed 1000-ohm resistance to ground, instead of the pot shown . . . AD7524 specifications: Under "Switching Characteristics," Chip Select to Write Setup Time is min (all versions) . . . 458/460 Data Sheet (8/81), page 3, and 1982 Databook, Volume II, page 12-19: Figure 3, Negative Input Signals, use a 5000-ohm, 50-ppm/°C resistor instead of a 500-ohm, 50-ppm/°C resistor for the full-scale adjust, R_S . . . AD2038 accuracies, data sheet (8/78), page 2, 1982 Databook, Volume II, page 16-50: For 590J/K/L, max specs are "Sensor calibrated @ +25°C, +3.2°C/+2.2°C/+1.8°C"; "Uncalibrated error @ +25°C, +5.2°C/+2.7°C/+1.2°C"; "Uncalibrated error (over range), +10.2°C/+5.7°C/+3.2°C." . . . AD2040 accuracies, data sheet (7/81), page 2, 1982 Databook, Volume II, page 16-52: For AD2626J/K/L, max specs are "Calibration error @ +25°C, +7.0°C/+4.5°C/+3.0°C"; Absolute error (over rated temp. range) "Without external calibration adjustment, +12.0°C/+7.5°C/+5.0°C"; "With +25°C calibration error set to zero, +5.0/+4.0/+3.6°C." . . . AD2009 Overrange output, data sheet (3/75), page 2, 1982 Databook, Volume II, page 16-20: Overrange output (pin 14) will be logic 1 (not logic 0) when the display count exceeds 1000 . . . Model 757 log-ratio amplifier, data sheet (9/81), page 4, 1982 Databook, Volume II, page 8-14: Maximum recommended input/output capacitance should be 33 pF (not 100 pF) . . . ADC1130/ADC1131, data sheet (6/77), page 4, 1982 Databook, Volume II, page 11-14, the correct mounting card is the AC1578 . . . DAC1423, data sheet (7/81), page 2, 1982 Databook, Volume II, page 10-28, pin diameter is 0.019 inches (0.48mm) . . . Models 290A, 292A, 1982 Databook, Volume II, page 5-28, shielded mounting socket is the ACI054 . . . Model 451, data sheet (12/80), page 1, 1982 Databook, Volume 2, page 12-11: minimum adjustable full-scale output frequency is 100 Hz (not 1 kHz) . . . Models 458/460, data sheet (8/81), page 3, Figure 3, 1982 Databook, Volume II, page 12-19, Figure 3: For negative signals only, use a 5000-ohm resistor for the full-scale adjustment . . . AC/DC Power-Supply Catalog (5/82): page 2: max load regulation is +0.02%; one-watt supplies equipped with pi filters are Models 958, 960, 962, and 964 (not 957, 959, 961, 963).

PATENTS . . . U. S. Patent 4,363,024, to A. Paul Brokaw, for "Digital-to-Analog Converter Providing Multiplicative and Linear Functions" . . . U. S. Patent 4,374,314, to James J. Deacutis, for "Laser Template Trimming of Circuit Elements."

The AD524. You can't build or buy a better I/A. And you won't believe the price—under $10!

The struggle to come up with the right I/A for your application is over. Never again will you have to design around two or three op amps and a handful of resistors, or pay the high price of a hybrid, or settle for a monolithic IC with less-than-satisfactory specs. Our new monolithic AD524 gives you all the performance and functionality you'll ever need in an I/A. And you can get it all at a price that's designed to make you forget the past.



The AD524 has the best specs attainable in an I/A, whether you're talking monolithic, hybrid, or discrete. Nonlinearity to ±0.003%. Input offset voltage drift of ±0.5 μV/°C. Gain error of ±0.02%. Common mode rejection of 130 dB. 0.3μV peak-to-peak low frequency noise. Your dream specs are now a reality!

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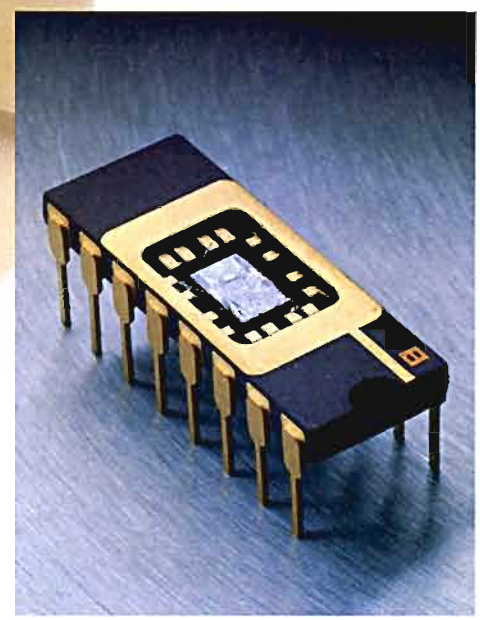
So if you're still rolling your own, or considering the National LM363 or the Burr-Brown INA101, find out just how good an instrumentation amp can be. Call Don Travers or Doug Grant today at 617-935-5565, or write Analog Devices, Inc., P.O. Box 280, Norwood, MA 02062.



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